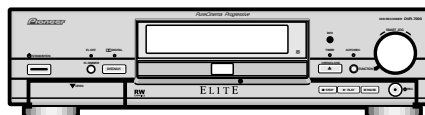


Service Manual



ORDER NO.
RRV2536

DVD RECORDER

DVR-7000

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Type	Model	Power Requirement	Region No.	Remarks
	DVR-7000			
KU/CA	○	AC120V	1	
LB	○	AC110V	3	

- For R/RW Recorder section, this service manual includes only EXPLODED VIEWS except Traverse Mechanism Assy-s, Block diagram and MAIN ASSY contrast table. For the detail of R/RW Recorder section, refer to the service manual for DVR-A03 (Order No. RRV2423).

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1. SAFETY INFORMATION

This service manual is intended for qualified service technicians ; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.

Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING

This product contains lead in solder and certain electrical parts contain chemicals which are known to the state of California to cause cancer, birth defects or other reproductive harm.

Health & Safety Code Section 25249.6 – Proposition 65

NOTICE

(FOR CANADIAN MODEL ONLY)

Fuse symbols  (fast operating fuse) and/or  (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE

(POUR MODÈLE CANADIEN SEULEMENT)

Les symboles de fusible  (fusible de type rapide) et/ou  (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

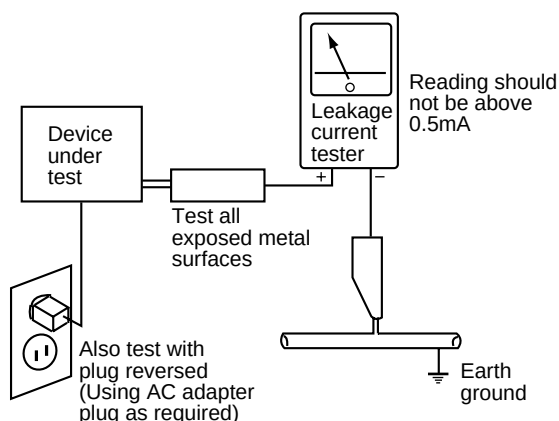
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a Δ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

IMPORTANT

THIS PIONNER APPARATUS CONTAINS LASER OF CLASS 1. SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

LASER DIODE CHARACTERISTICS

MAXIMUM OUTPUT POWER : 35 mw
WAVELENGTH : 658 nm

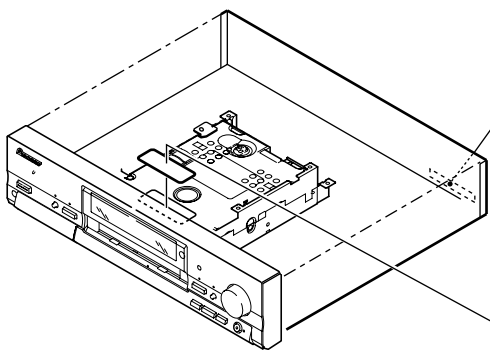
WARNING!

DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.



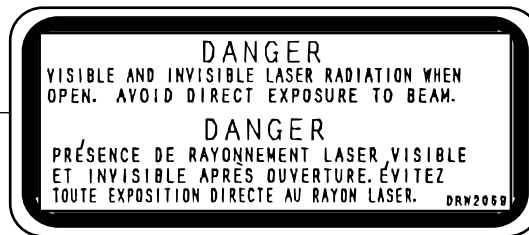
LASER
Picture 1
Warning sign for laser radiation

■ LABEL CHECK



DANGER
VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN.
AVOID DIRECT EXPOSURE TO BEAM.

Printed on Rear Panel



DRW2069

Additional Laser Caution

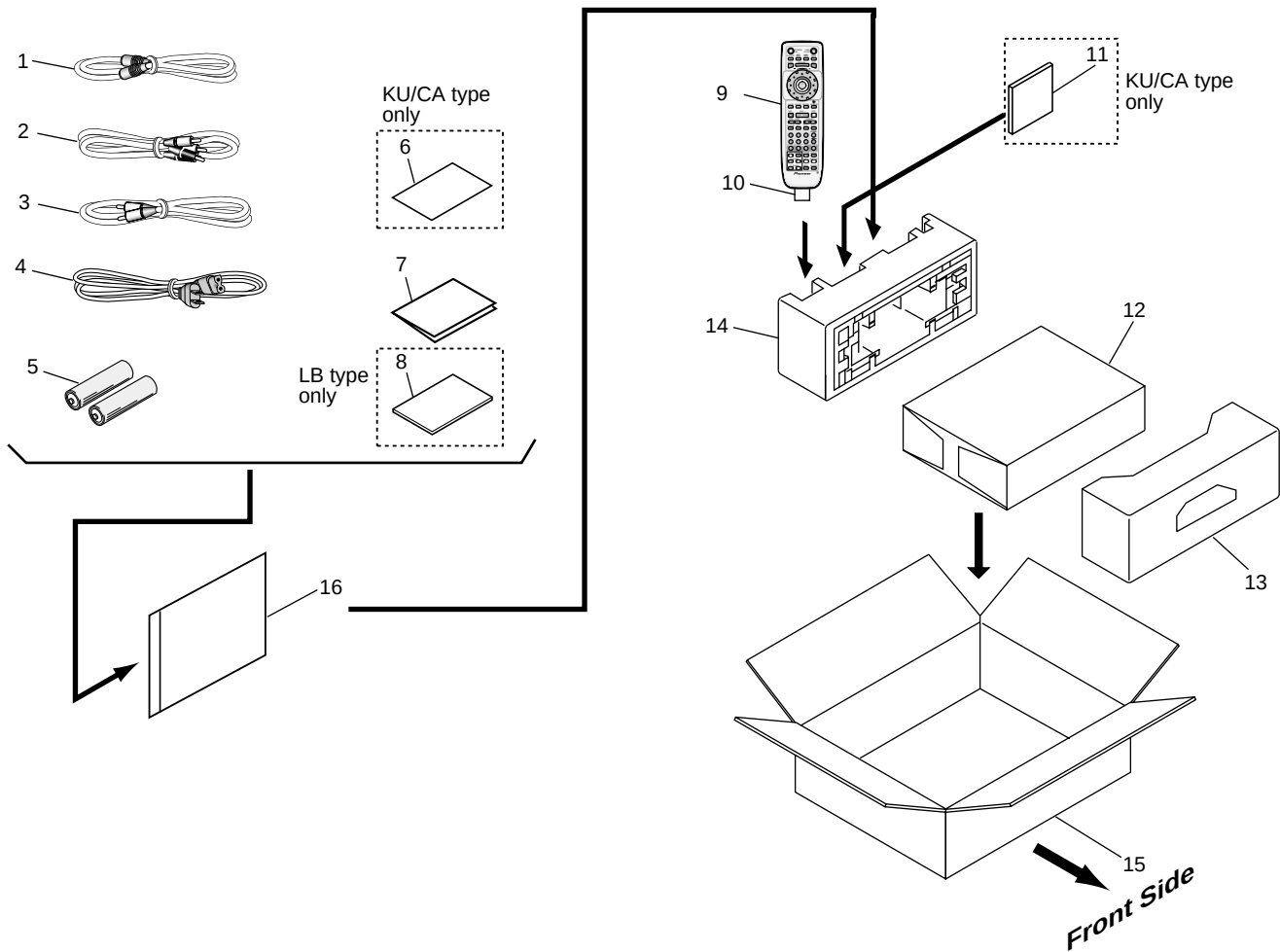
1. The ON/OFF(ON:low level,OFF:high level) status of the CLAMP signals for detecting the loading state are detected by the drive CPUs, and the design prevents laser diode oscillation when the CLAMP signal turns OFF. In normal operation, if no disc is clamped, the laser diode oscillation is disabled. However, the interlock does not always operate in the test mode. *
2. When the cover is opened, close viewing of the objective lens with the naked eye will cause exposure to a Class 3A laser beam.

* Refer to pages 43 of DVR-A03 Service Manual(RRV2423).

2. EXPLODED VIEWS AND PARTS LIST

NOTES: ● Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.
 ● The  mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
 ● Screws adjacent to ▼ mark on product are used for disassembly.

2.1 PACKING



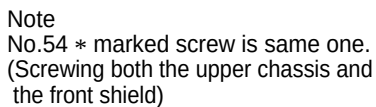
(1)PACKING PARTS LIST

Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	1	RF Antenna Cable	VDE1025	NSP	11	DVD-RW Disc Ver.1.1	See Contrast table (2)
	2	Stereo Audio Cable	VDE1033		12	Mirror Sheet	VHL1006
	3	Video Cable	VDE1034		13	Front Pad (PS)	VHA1275
△	4	AC Power Cord	ADG7021		14	Rear Pad (PS)	VHA1276
NSP	5	Battery (R6P,AA)	VEM-013		15	Packing Case	See Contrast table (2)
NSP	6	Warranty Card	See Contrast table (2)	NSP	16	Polyethylene Bag (230×340×0.03)	Z21-038
	7	Operating Instructions	See Contrast table (2)				
	8	Operating Instructions	See Contrast table (2)				
	9	Remote Control Unit	See Contrast table (2)				
	10	Battery Cover	VNK4828				

(2) CONTRAST TABLE

DVR-7000/KU/CA and DVR-7000/LB are constructed the same except for the following:

Mark	No.	Symbol and Description	Part No.		Remarks
			DVR-7000/KU/CA	DVR-7000/LB	
NSP	6	Warranty Card	ARY1026	Not used	
	7	Operating Instructions (English)	VRB1275	VRB1280	
	8	Operating Instructions (Chinese)	Not used	VRE1095	
	9	Remote Control Unit	VXX2763	VXX2777	
NSP	11	DVD-RW Disc Ver1.1	VZZ1001	Not used	
	15	Packing Case	VHG2122	VHG2152	



(1) EXTERIOR PARTS LIST

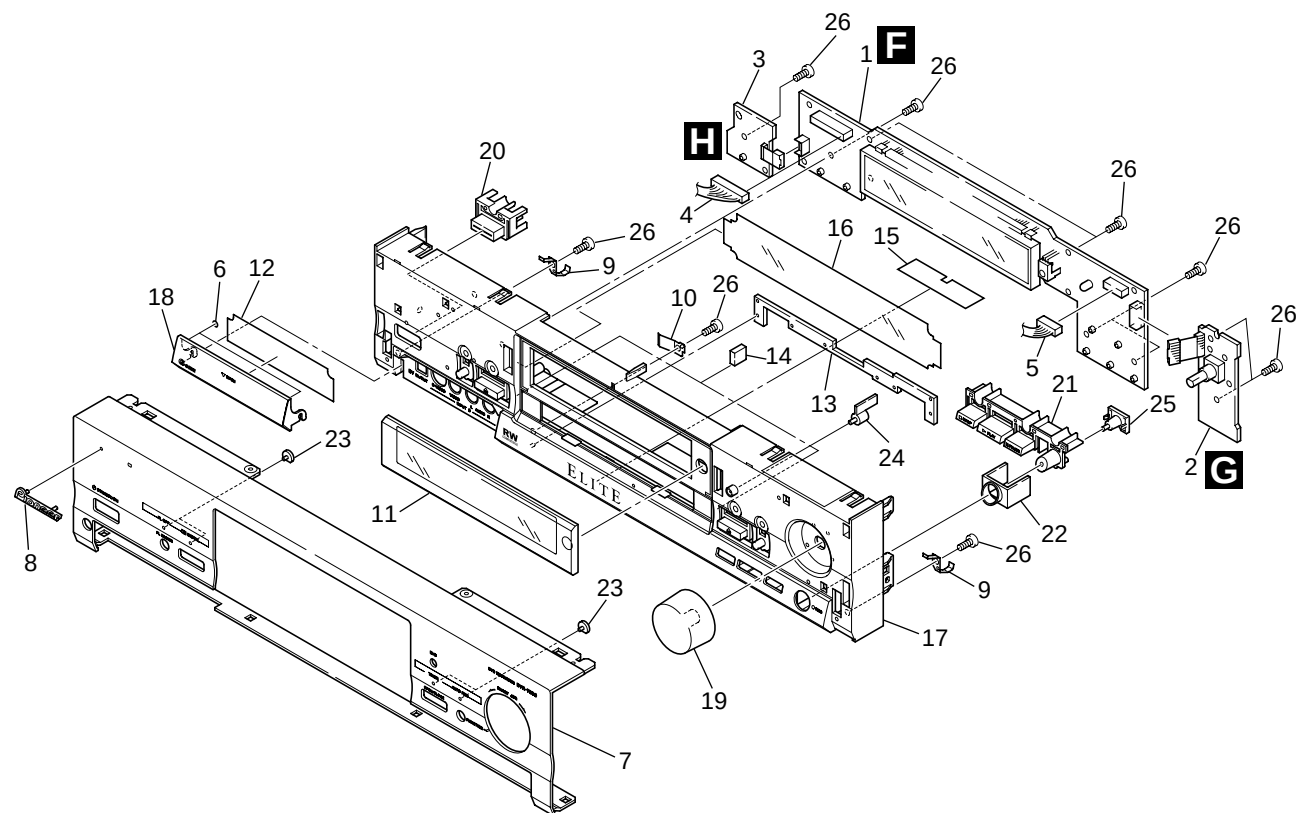
Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	1	TUMJ ASSY	VWV1885	NSP	39	Shield Case(MTL)	VNE2260
	2	REAR JACK ASSY	VWV1887	NSP	40	Plate(MTL)	VNE2265
	3	3D Y/C ASSY	VWV1888		41	Insulator(ABS)	VXA2424
	4	FRONT JACK ASSY	VWV1886		42	DVD Badge(PC)	VAM1119
	5	MAIN ASSY	VWV1894		43	Tray Spring(BK)	VBH1337
△	6	POWER SUPPLY ASSY	VWR1347		44	Tray Spacer	VEC2239
	7	DVD-R/RW UNIT	DVR-103-PA		45	Tray Cushion S	VEC2263
	8	Connector Assy (MAIN ASSY CN2003 ↔POWER ASSY CN201)	PF14PP2S30		46	Tray Panel(ABS)	VNK4801
	9	Connector Assy (TUMJ ASSY CN2001 ↔POWER ASSY CN202)	PF16PP2S30	NSP	47	Tray Holder(ABS)	VNK4809
	10	Flexible Cable(20P) (TUMJ ASSY CN2010 ↔MAIN ASSY CN2001)	VDA1875		48	ID Label	VRW1877
	11	Flexible Cable(22P) (TUMJ ASSY CN1003 ↔MAIN ASSY CN7001)	VDA1876		49	Binder	PEC-107
	12	Housing Assy(6P) (FRONT-J ASSY CN2004 ↔MAIN ASSY CN9001)	VKP2263		50	Screw(Steel)	ABA7008
	13	Housing Assy(10P) (TUMJ ASSY CN3001 ↔MAIN ASSY CN8001)	VKP2264		51	Screw(Steel)	VBA1082
	14	DC FAN Motor	VXM1092		52	HLS Screw(Steel)	ABA7029
NSP	15	Locking Wire Saddle	DEC1305		53	Screw	BBZ26P050FMC
	16	Wire Saddle	DEC1450		54	Screw	BBZ30P060FMC
NSP	17	Card Spacer	DEC1772		55	Screw	BPZ30P080FZK
	18	Stick Finger	DNB1092		56	Screw	FBT40P080FNI
NSP	19	P.Plate Holder	PNY-405		57	•••••	
	20	Earth Plate(Cu)	VBK1070		58	FFC Cable(40P) (MAIN ASSY CN3001↔ RECORDER DRIVE MAIN CN409)	DDD1192
	21	Earth Metal(Cu)	VBK1094		59	Housing Assy(6P) (MAIN ASSY CN6001↔ RECORDER DRIVE MAIN CN407)	DKP3550
	22	Cooling Sheet (23×23)	VEB1332		60	Housing Assy(4P) (MAIN ASSY CN2002↔ RECORDER DRIVE MAIN CN406)	DKP3551
	23	Card Spacer	VEC1708		61	Connector Assy (POWER ASSY CN203↔ RECORDER DRIVE MAIN CN403)	PF06PP2S42
	24	Spacer	VEC2157		62	Coolig Sheet S	VEB1333
	25	Locking Card Spacer	VEC2234		63	Gasket	VEC2235
	26	Dust Spacer A	VEC2237		64	Gasket(L)	VEC2252
	27	Dust Spacer B	VEC2238		65	Gasket(M)	VEC2253
	28	Barrier Sheet(PPE)	VEC2251		66	Gasket(T)	VEC2267
	29	Dust Spacer C	VEC2261		67	Gasket(N)	VEC2273
	30	Spacer	VEC2262		68	Front Shield(MTL)	VNE2261
NSP	31	Wire Saddle(5S)	VEC2270		69	65 Label	See Contrast table (2)
NSP	32	Chassis(FE)	VNA2277		70	Fuse Caution Label	See Contrast table (2)
	33	Rear Panel(FE)	See Contrast table (2)		71	Fuse Caution Label	See Contrast table (2)
	34	Bonnet(FE)	VXX2814				
NSP	35	Upper Frame(FE)	VNE2244				
NSP	36	Input Plate	VNE2245				
NSP	37	Upper Plate Assy	VNE2272				
NSP	38	Upper Chassis(MTL)	VNE2259				

(2) CONTRAST TABLE

DVR-7000/KU/CA and DVR-7000/LB are constructed the same except for the following:

Mark	No.	Symbol and Description	Part No.		Remarks
			DVR-7000/KU/CA	DVR-7000/LB	
	33	Rear Panel	VNA2328	VNA2329	
	69	65 Label	ARW7050	Not used	
	70	Fuse Caution Label	VRW1902	Not used	
	71	Fuse Caution Label	VRW1903	Not used	

2.3 FRONT PANEL



(1)FRONT PANEL PARTS LIST

Mark	No.	Description	Part No.
	1	FL ASSY	VWG2314
	2	JOG ASSY	VWG2316
	3	SW ASSY	VWG2315
	4	Flexible Cable(20P) (FL ASSY CN1202↔ TUMJ ASSY CN2009)	VDA1874
	5	Connector Assy (FL ASSY CN1201↔ POWER ASSY CN204)	PF07PP2S17
	6	Cushion Rubber	AEB7068
	7	Front Aluminium(AL)	See Contrast table (2)
	8	Pioneer Badge(AL)	VAM1124
	9	Earth Plate(Cu)	VBK1133
	10	Door Spring(SUS)	VBK1134
	11	FL Window(PMMA)	VEC2197
	12	Input Sheet(PC)	VEC2199
	13	Drive Sheet(EPDM)	VEC2275
	14	Drive Cushion	VEC2258
	15	Drive Filter	VEC2259
	16	FL Filter(PC)	VEC2260
	17	Panel Base(ABS)	See Contrast table (2)
	18	Input Door(ABS)	See Contrast table (2)
	19	Dial Knob(ABS)	VNK4802
	20	Power Button(ABS)	VNK4803
	21	Play Button(ABS)	VNK4804
	22	Record Ring(ABS)	VNK4805
	23	Combined Lens(MMA/BS)	VNK4806
	24	DVD Lens(MMA/BS)	VNK4807
	25	Record Lens(MMA/BS)	VNK4827
	26	Screw	BPZ30P080FZK

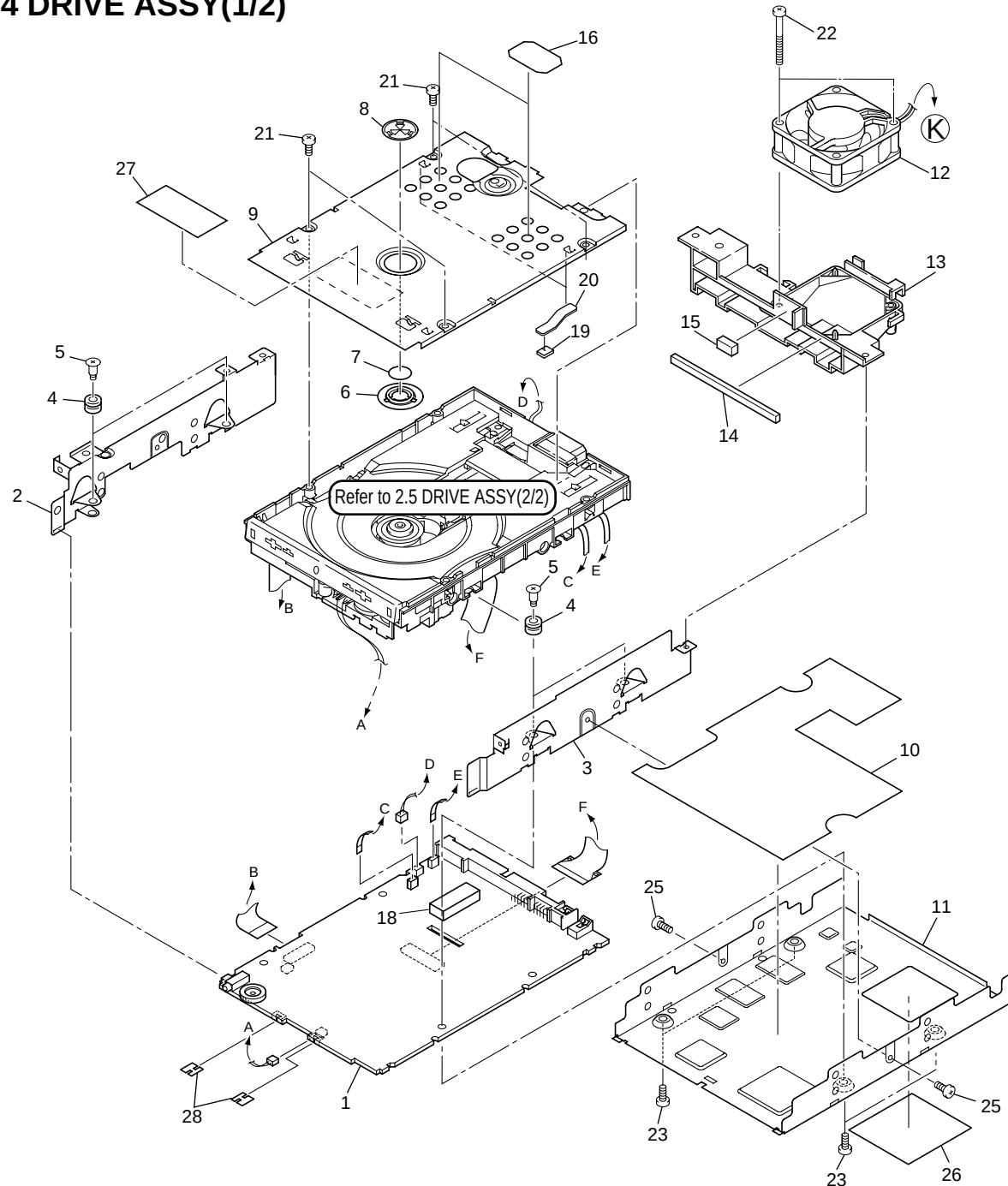
(2) CONTRAST TABLE

DVR-7000/KU/CA and DVR-7000/LB are constructed the same except for the following:

Mark	No.	Symbol and Description	Part No.		Remarks
			DVR-7000/KU/CA	DVR-7000/LB	
	7	Front Aluminium(AL)	VAH1392	VAH1378	
	17	Panel Base(ABS)	VNK4983	VNK4799	
	18	Input Door(ABS)	VNK4924	VNK4800	

DVR-7000

2.4 DRIVE ASSY(1/2)

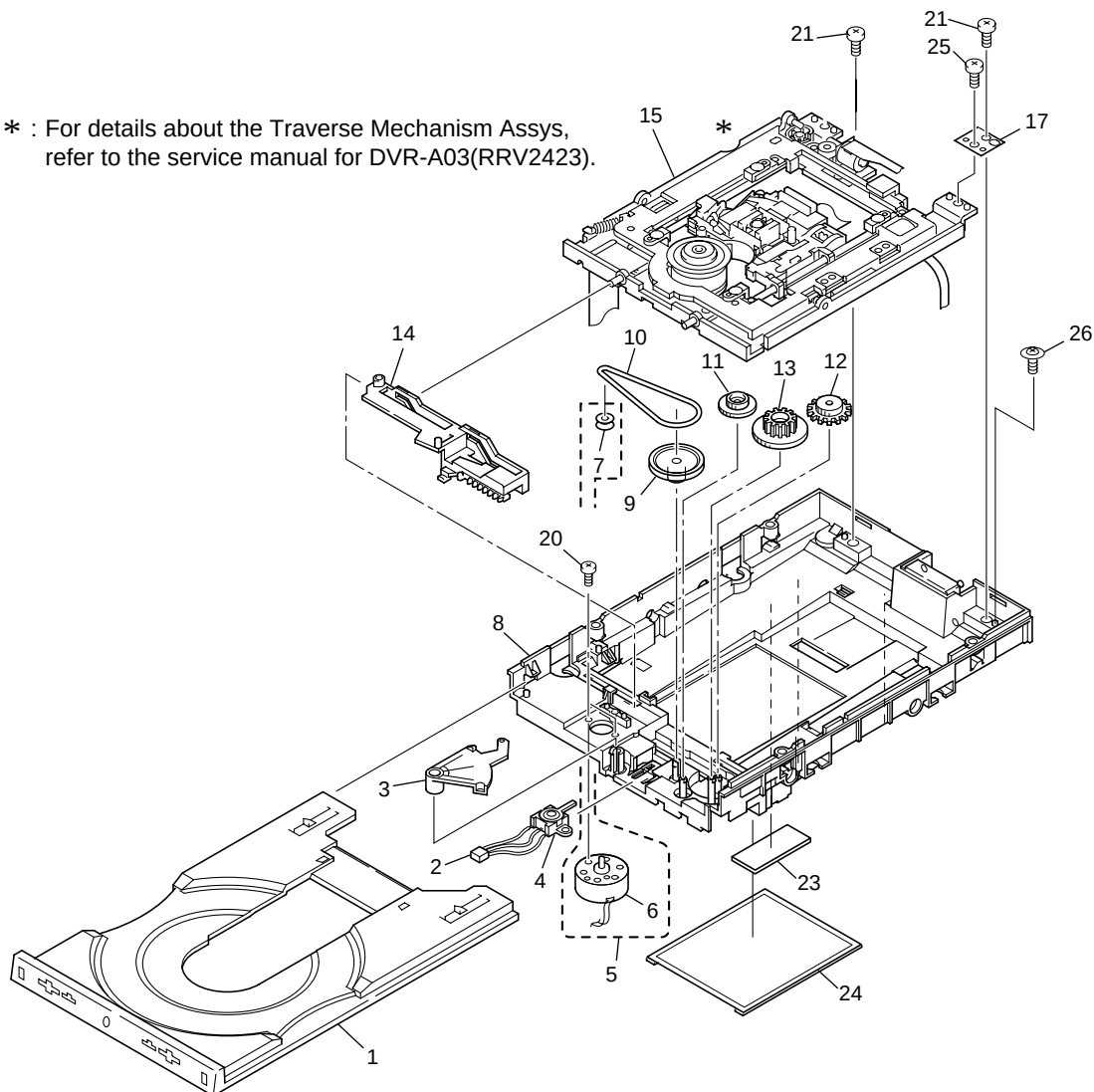


● DRIVE ASSY(1/2) PARTS LIST

Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	1	RECORDER DRIVE MAIN	DWX2148		15	Duct Seal B	VEC2209
NSP	2	Flame L	VNE2242	NSP	16	Dust Sheet	VEC2236
NSP	3	Flame R	VNE2243		17	•••••	
	4	Float Rubber	DEB1466		18	Air Cushion	DEB1488
	5	Float Screw	DBA1148		19	Spacer POR	DEB1483
	6	Clamper	DNK3829		20	Plate	DNK3839
	7	Clamper Yoke	DNH2467		21	Screw	BPZ26P060FZK
	8	Upper Clamper	DNK3830		22	Screw	BPZ30P350FZK
	9	Clamper Holder	DNC1548		23	Screw	PMA26P060FMC
	10	Radiate Sheet	DEB1473		24	•••••	
	11	Base Chassis	DNC1549		25	Screw	DBA1159
	12	DC Fan Motor	AXM7014		26	Label	DRW2053
NSP	13	Fan Duct	VNK4796		27	Caution Label	DRW2069
	14	Duct seal A	VEC2208		28	Acetate Tape	DEH1021

2.5 DRIVE ASSY(2/2)

* : For details about the Traverse Mechanism Assys,
refer to the service manual for DVR-A03(RRV2423).



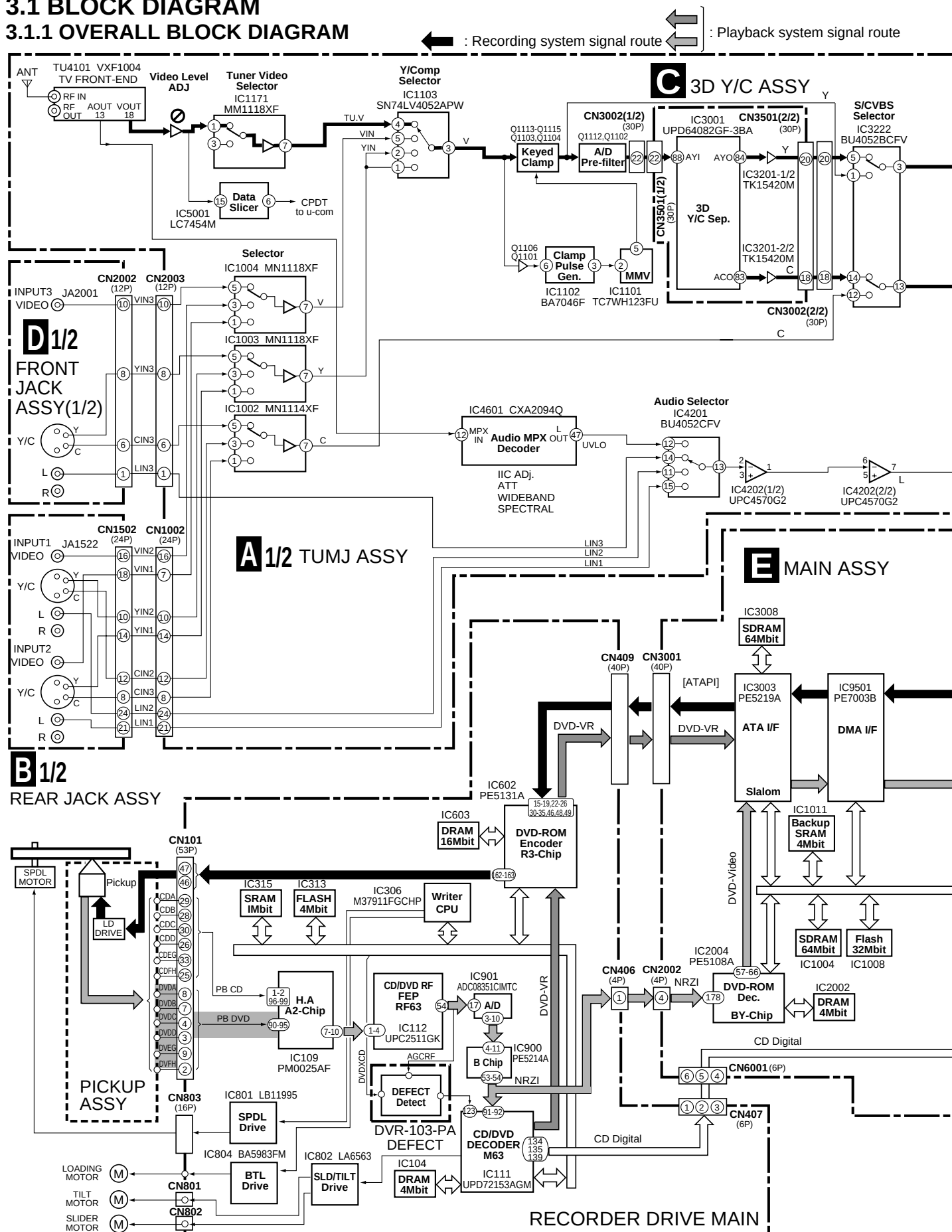
● DRIVE ASSY(2/2) PARTS LIST

Mark	No.	Description	Part No.	Mark	No.	Description	Part No.
	1	Tray	VNK4808		16		
	2	Connector Assy(3P)	DKP3544		17	Plate	DBK1208
	3	Eject Lever	DNK3817		18		
	4	Lever Switch	DSK1001		19		
	5	Loading Motor Assy-s	DXX2491		20	Screw	JGZ17P030FMC
NSP	6	Carriage Motor	RXM1090		21	Screw	BPZ26P060FZK
	7	Motor Pulley	PNW1634		22		
NSP	8	Loading Base	DNK3811		23	Air Cushion	DEB1488
	9	Gear Pulley	DNK3813		24	Sheet (Rubber)	DEC2411
	10	Belt (Rubber)	DEB1465		25	Screw	BMZ26P050FMC
	11	Gear A	DNK3814		26	Screw	VBA1034
	12	Gear C	DNK3816				
	13	Gear B	DNK3815				
NSP	14	Clamp Cam	DNK3818				
NSP	15	Traverse Mechanism Assy-s	DXB1744				

3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM

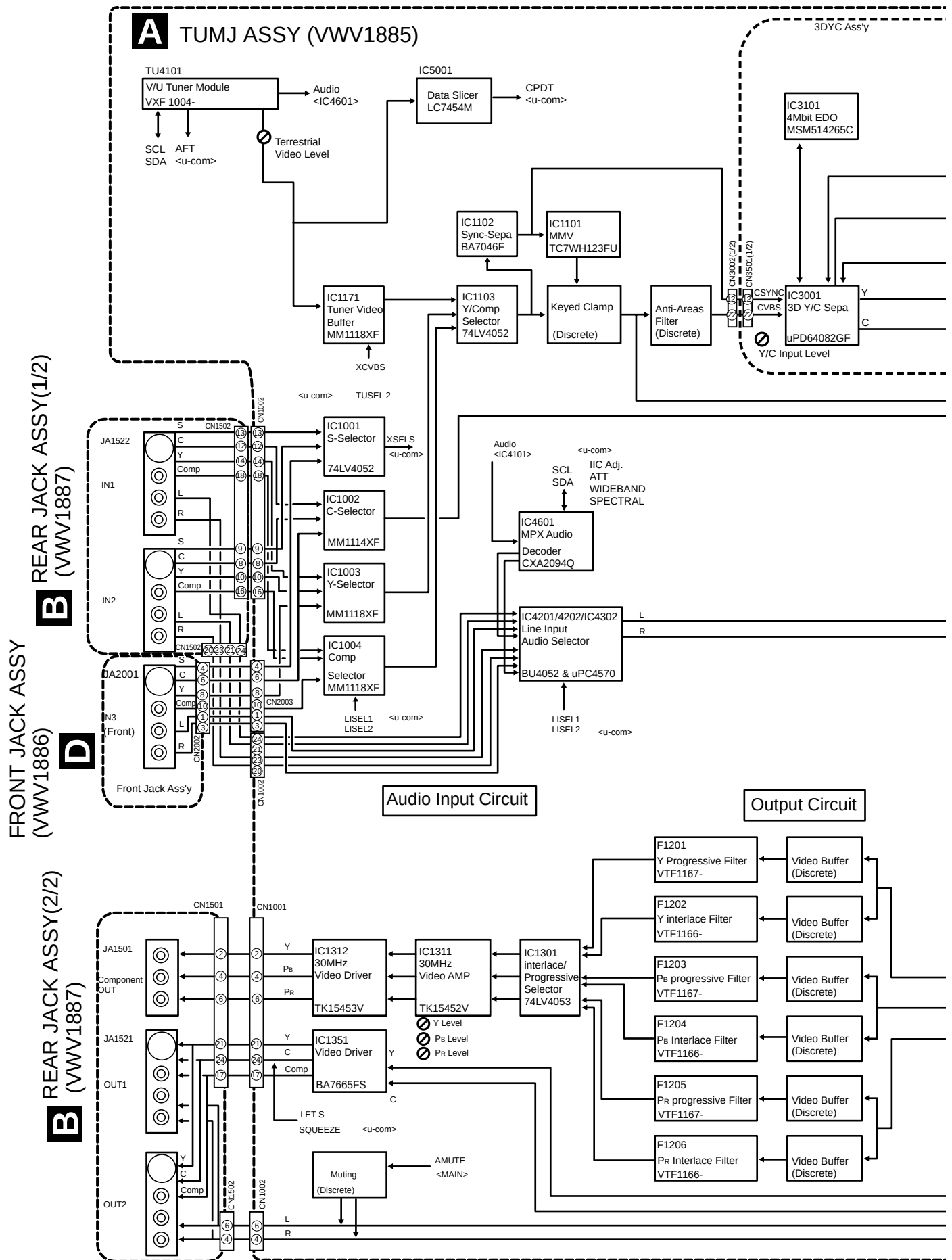
3.1 BLOCK DIAGRAM

3.1.1 OVERALL BLOCK DIAGRAM

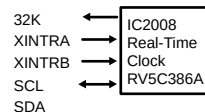
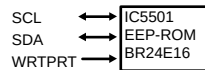
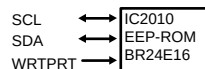
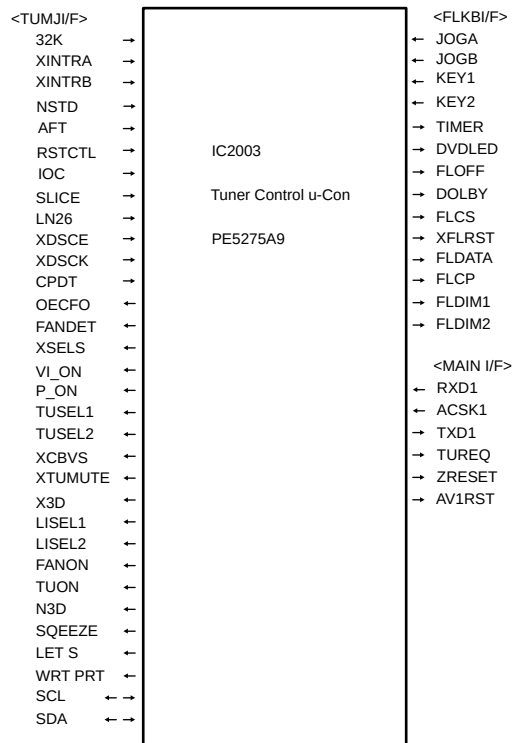
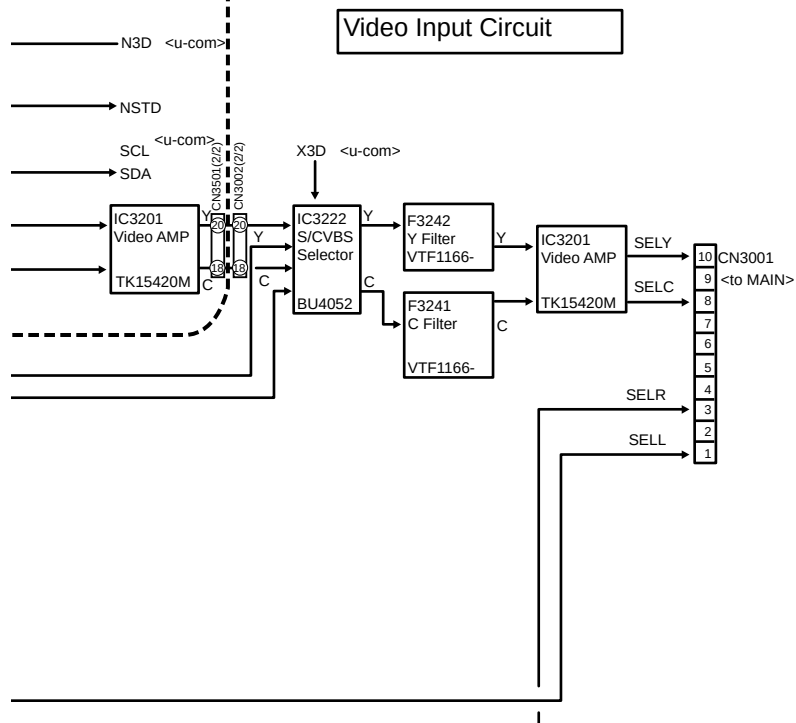




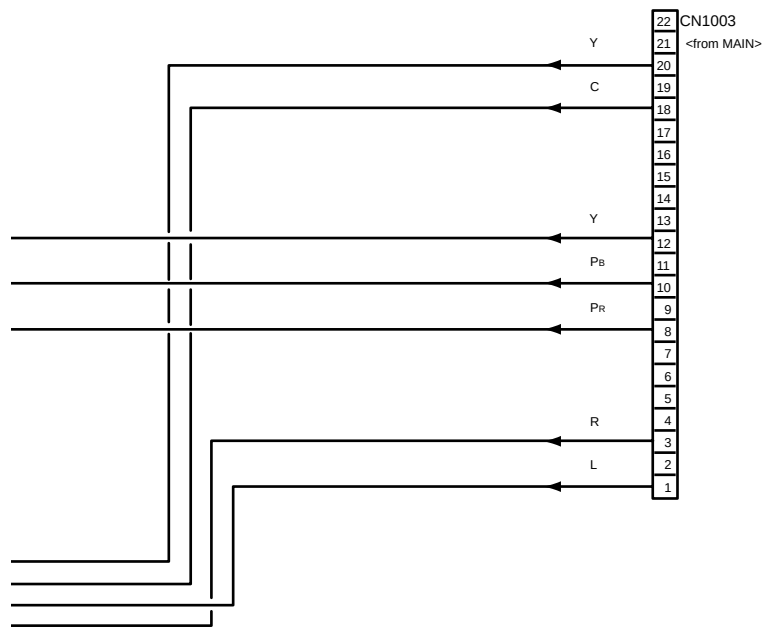
3.1.2 TUJB ASSY BLOCK DIAGRAM



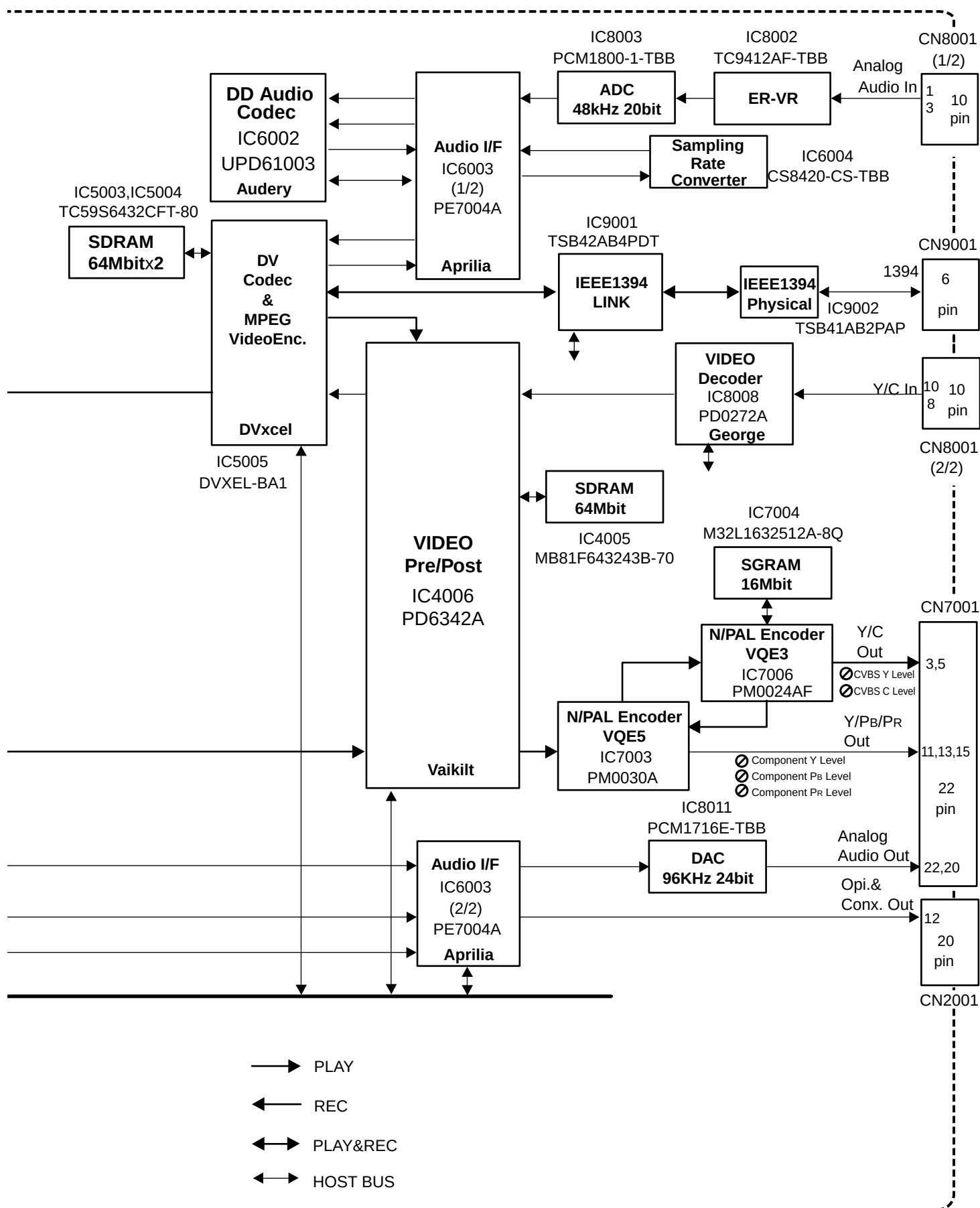
C 3D Y/C ASSY (VWV1888)



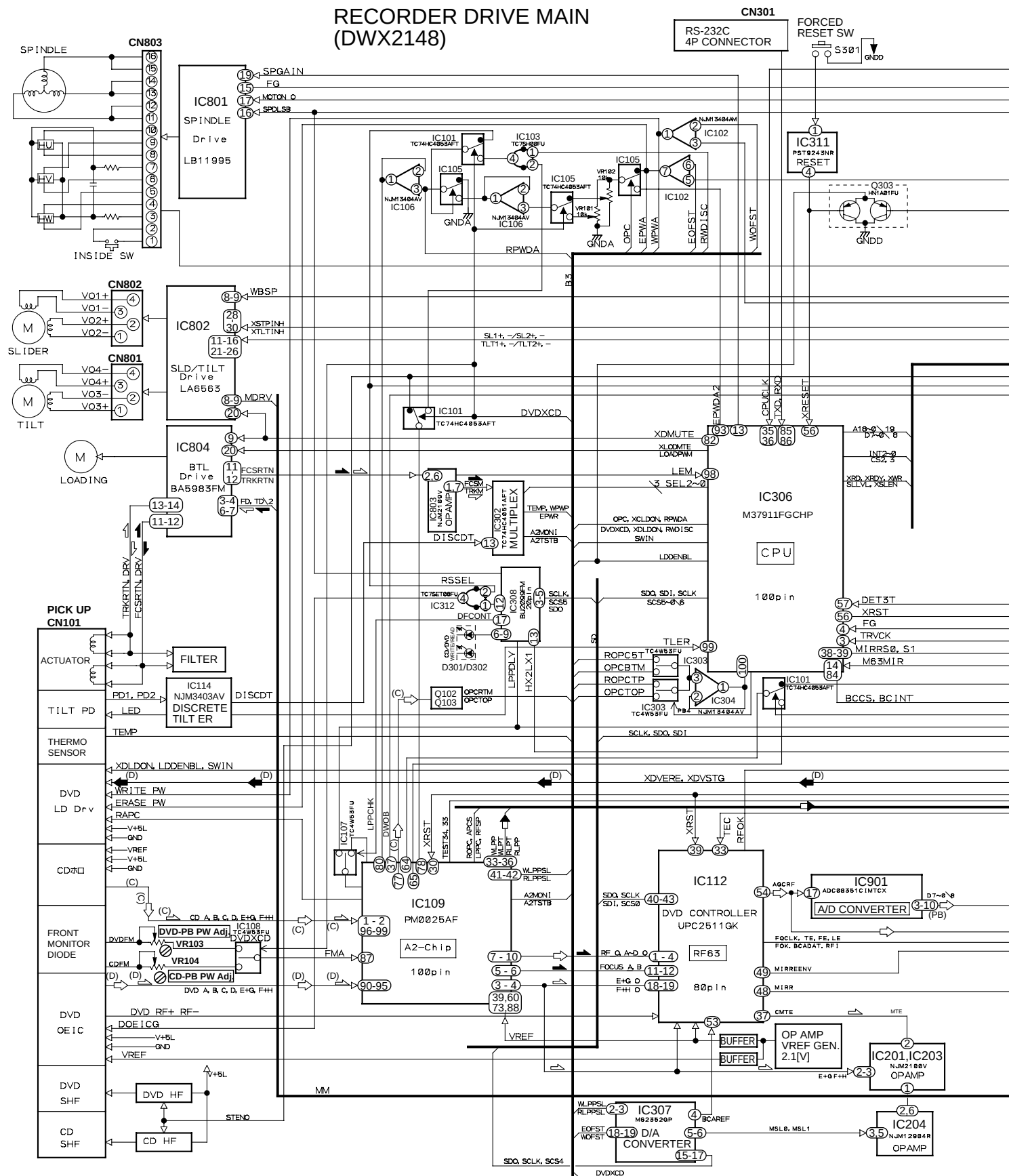
u-com I/F

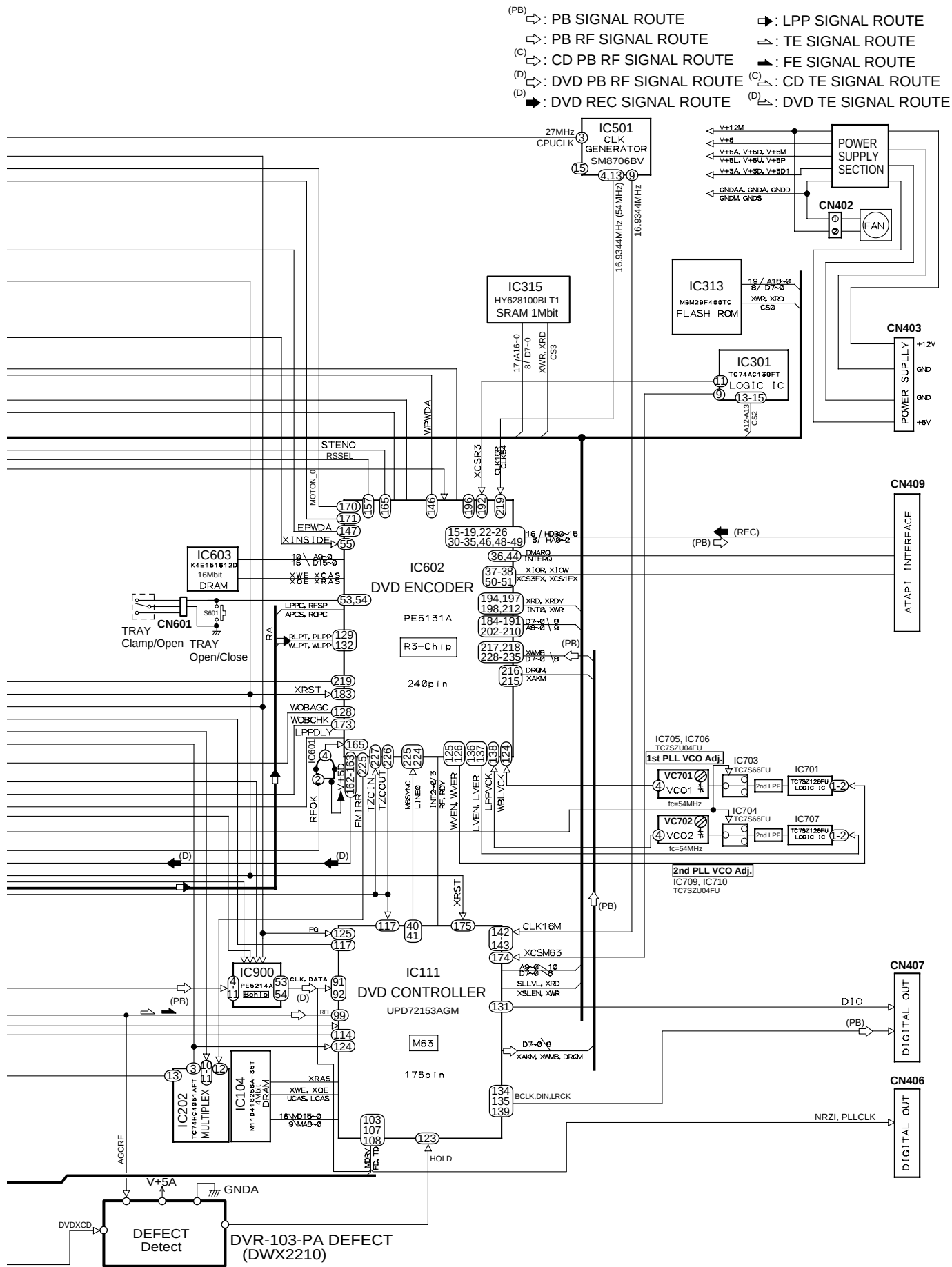




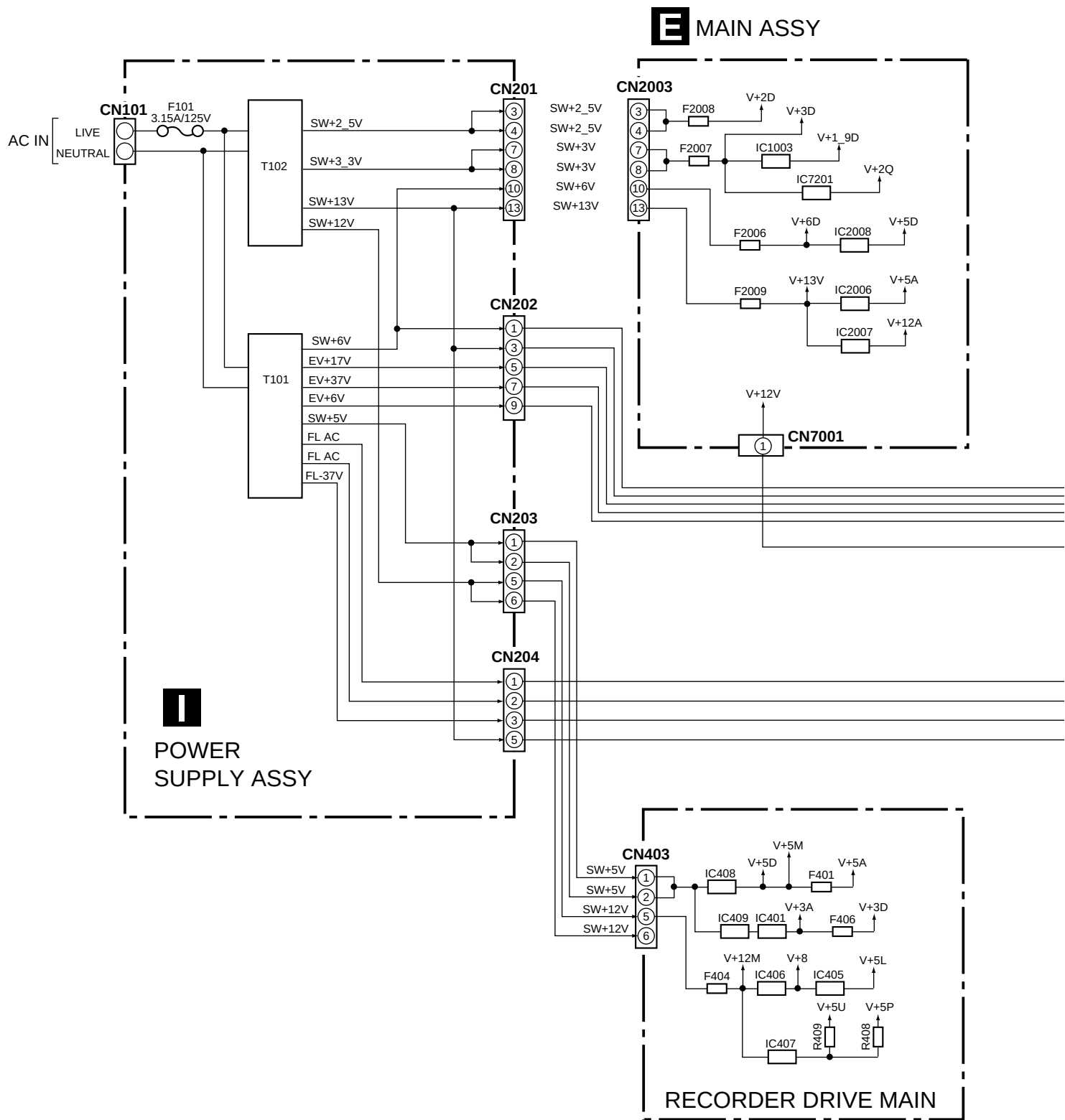


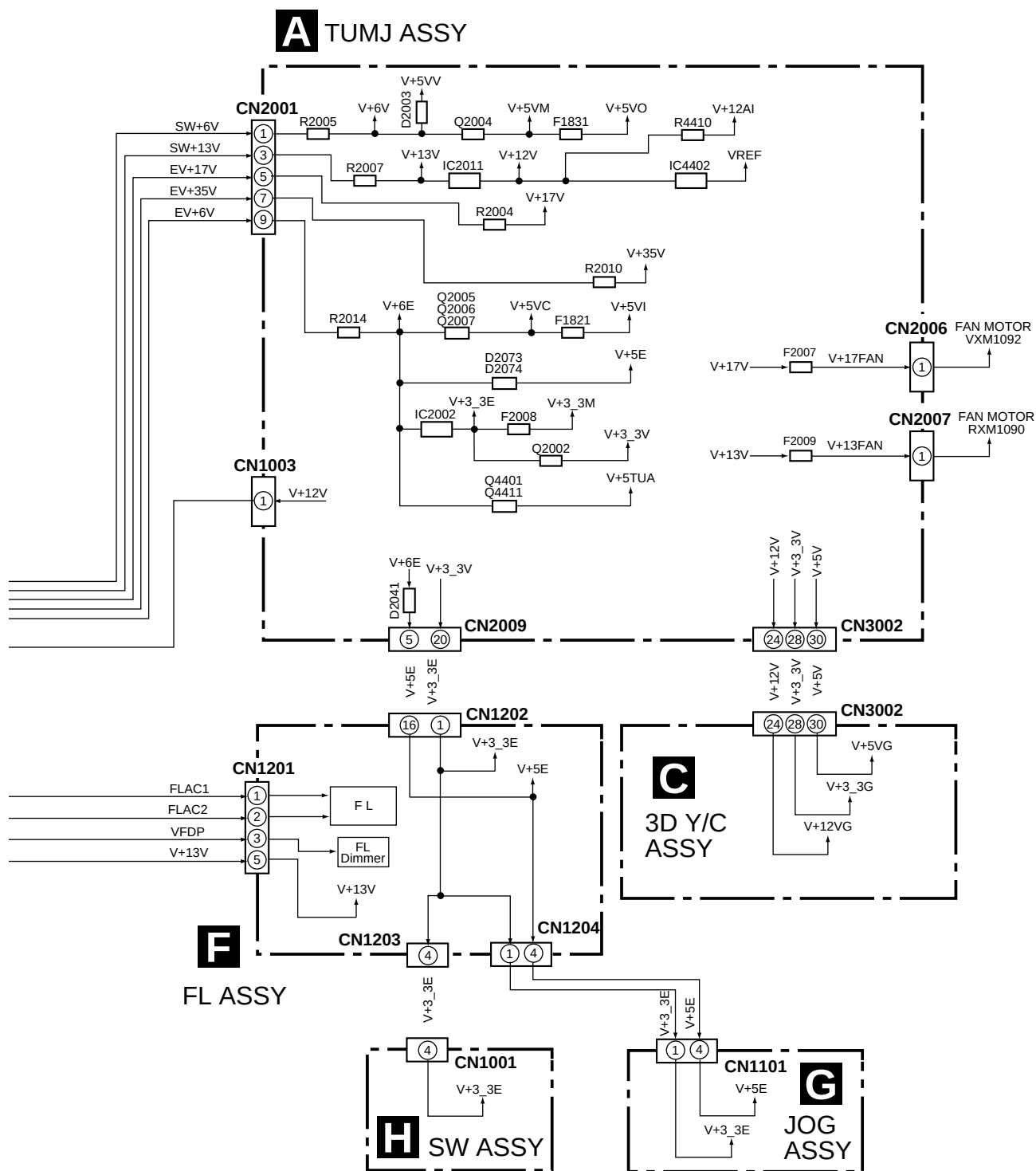
3.1.4 RECORDER DRIVE MAIN BLOCK DIAGRAM



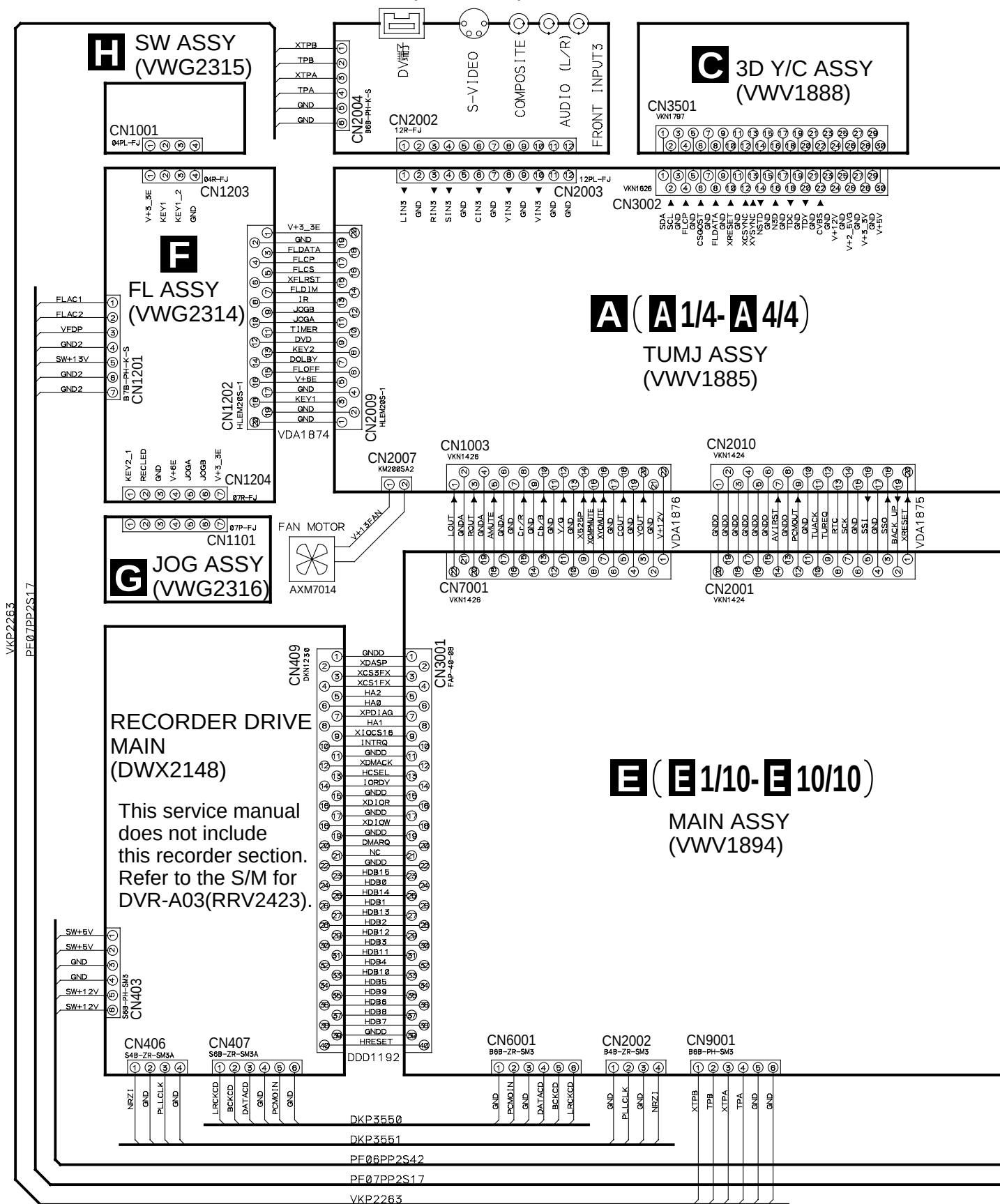


3.1.5 POWER BLOCK DIAGRAM

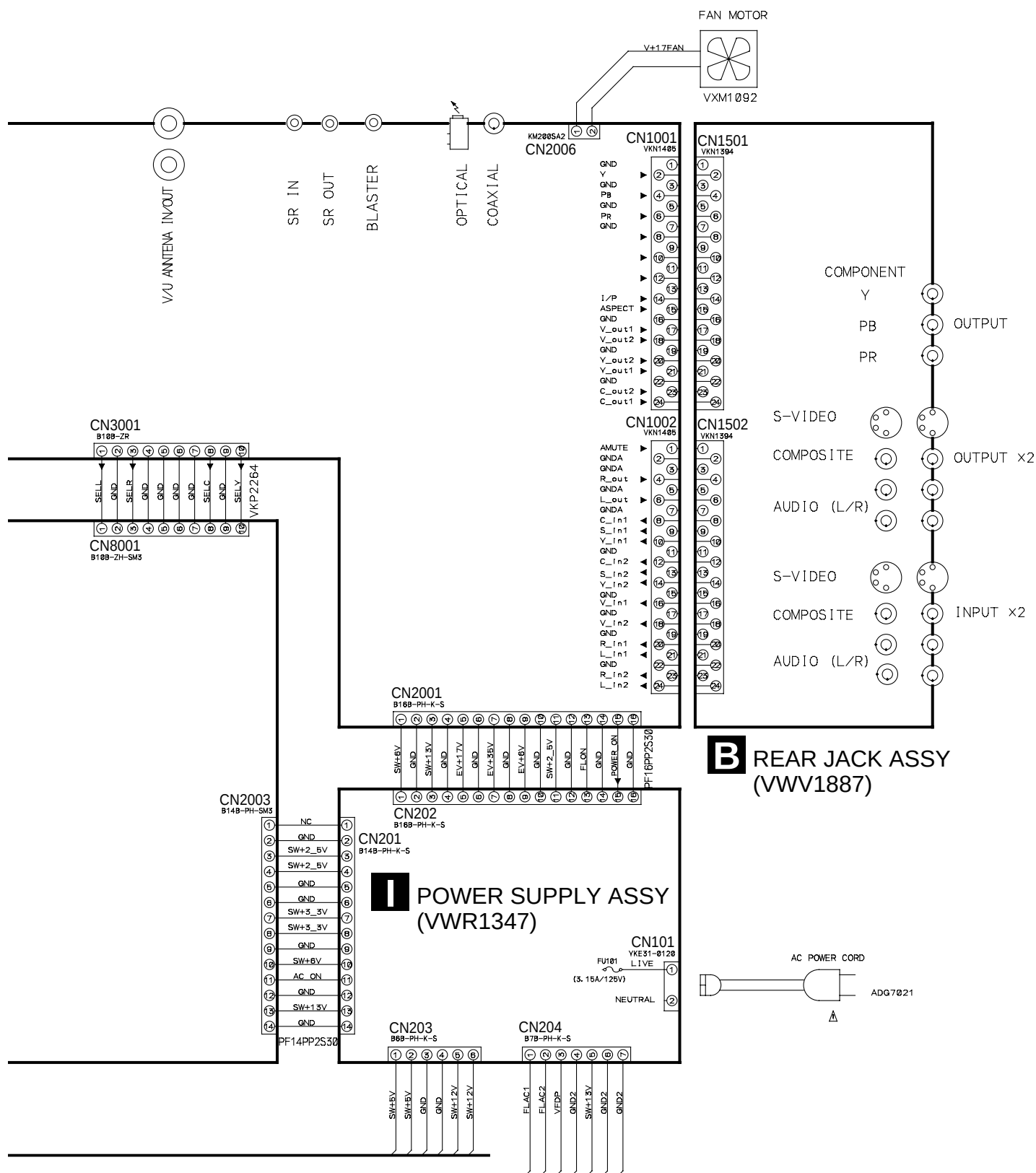




D FRONT JACK ASSY
(VWV1886)



Note : When ordering service parts, be sure to refer to "EXPLODED VIEWS and PARTS LIST" or "PCB PARTS LIST".





C

D



A 2/4



8

3.5 TUMJ ASSY(3/4) and 3D Y/C ASSY

A 3/4 TUMJ ASSY
(VWV1885)

- NOTE

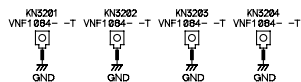
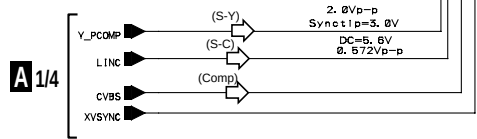
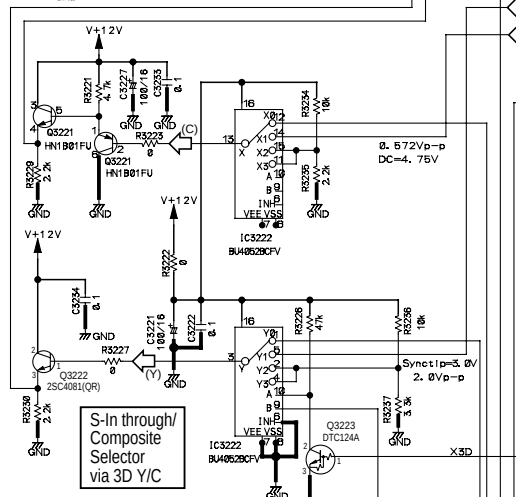
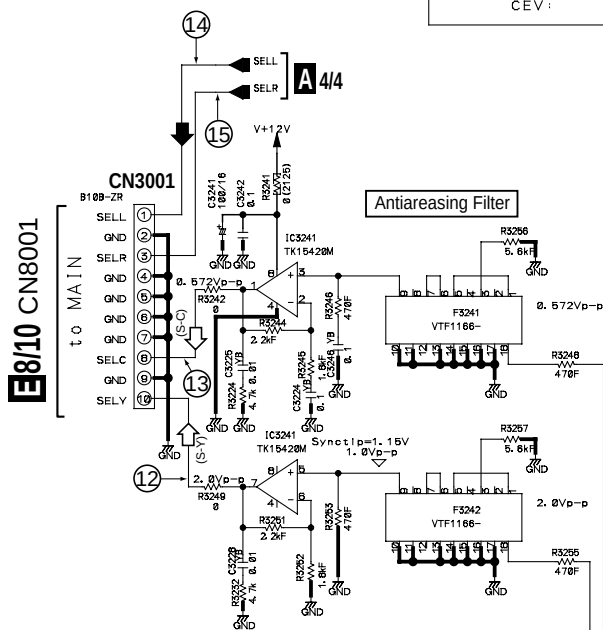
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 R without notice RS1/16S***J
 F : RS1/16SF
 *** (2125) : RS1/10S***J

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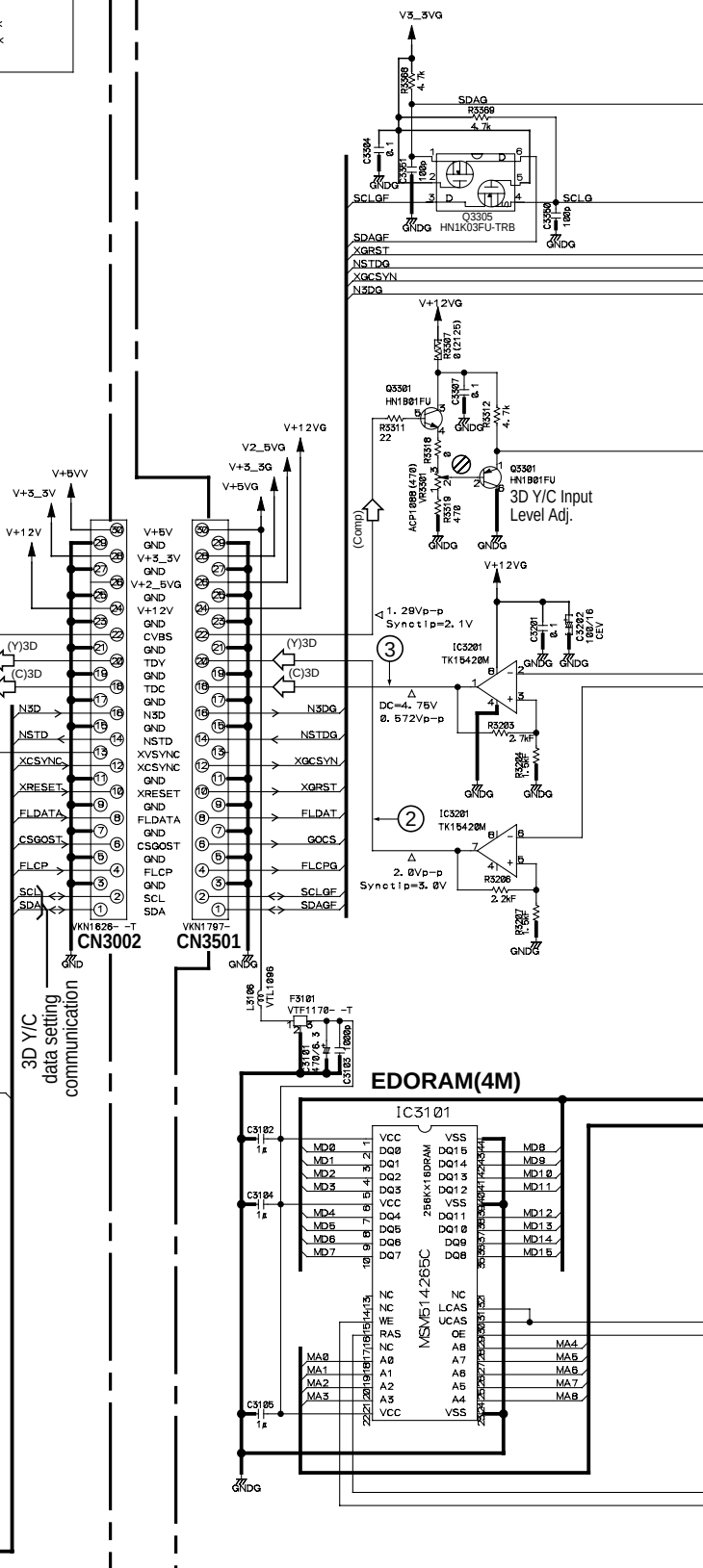
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 JQ: CEJQ***
 CEV: CEV***



CPU CONTROL BUS (to 2/4)

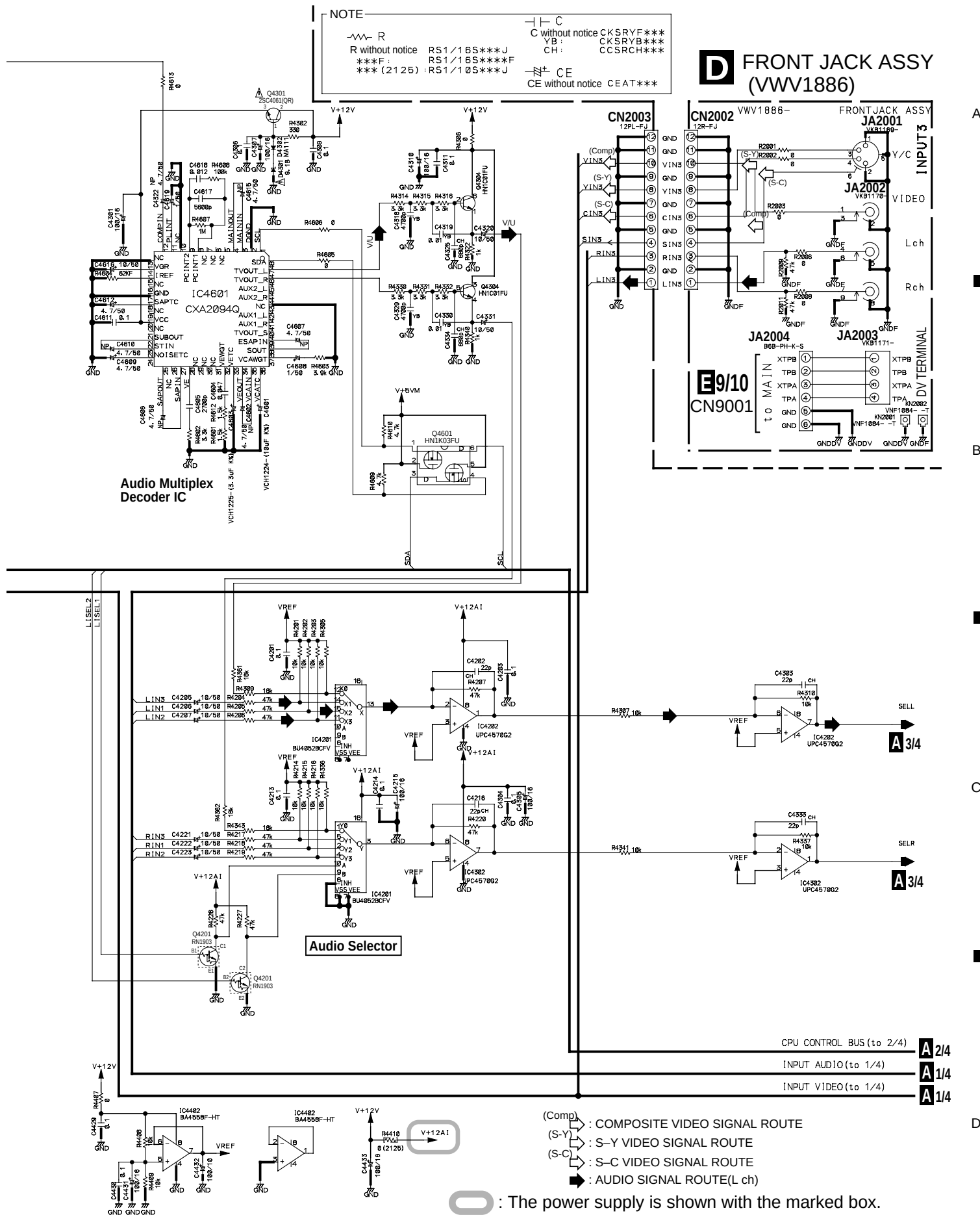


A

- B



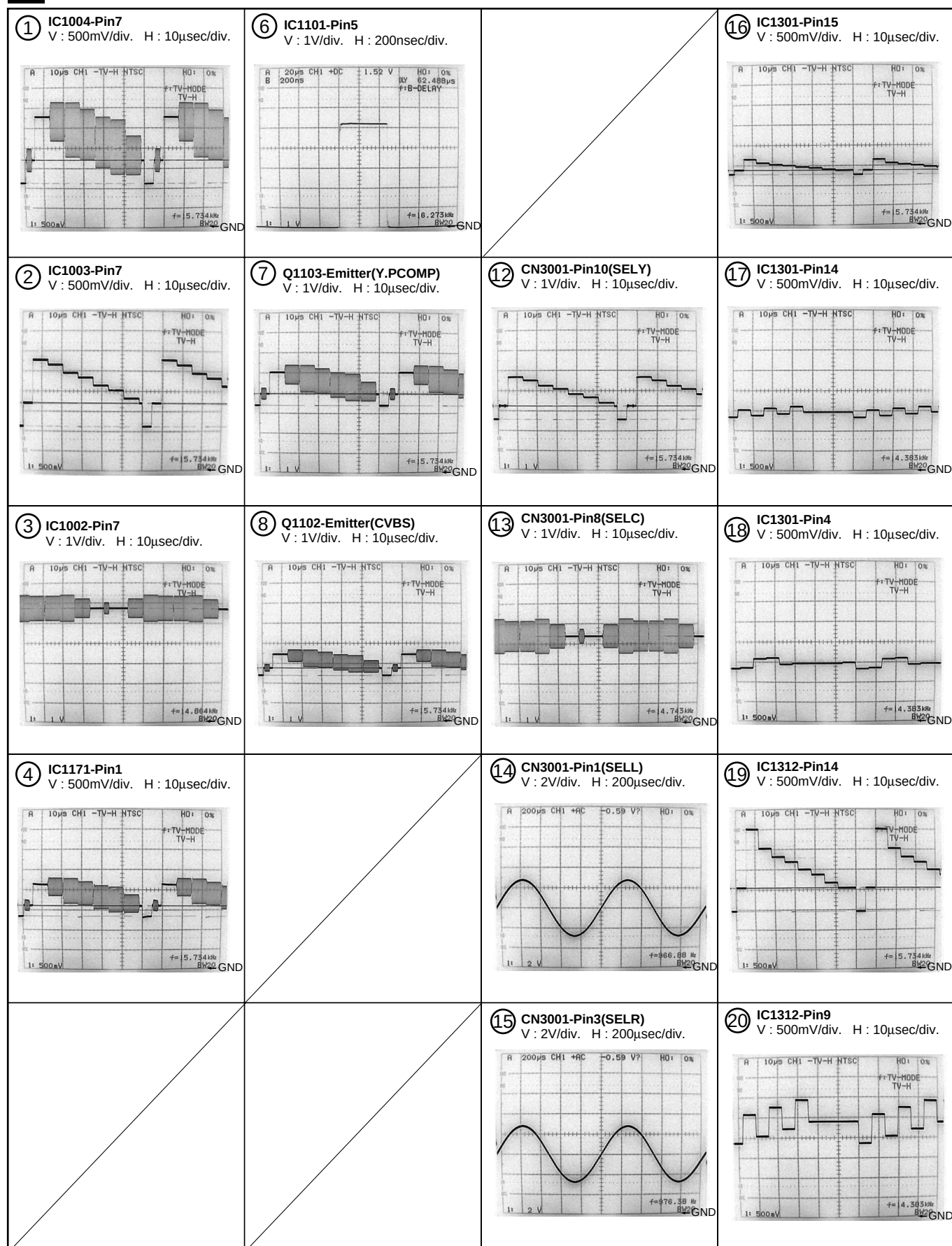
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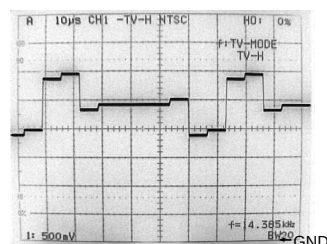
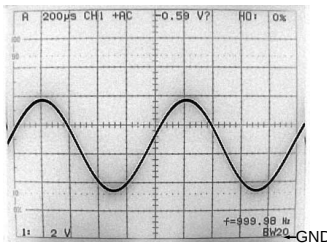
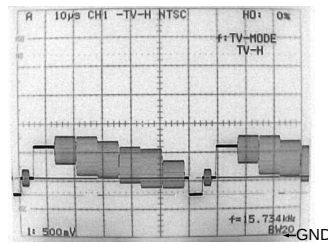
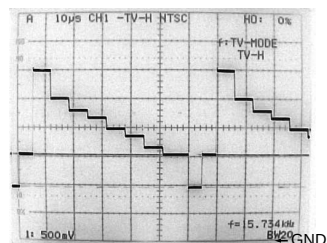
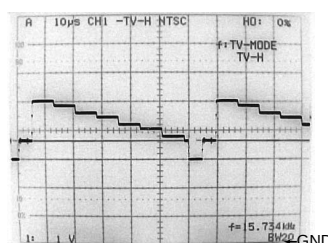
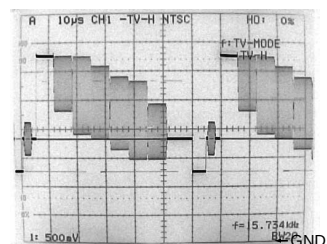
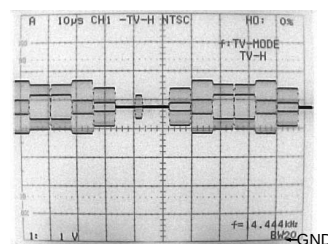
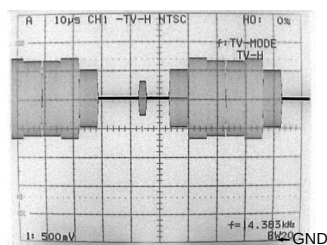
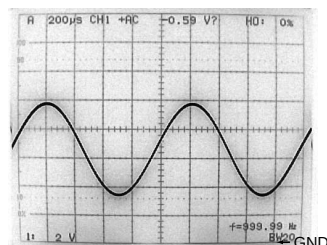


WAVEFORMS

Note : The encircled numbers denote measuring point in the schematic diagram.

A TUMJ ASSY(1/2)

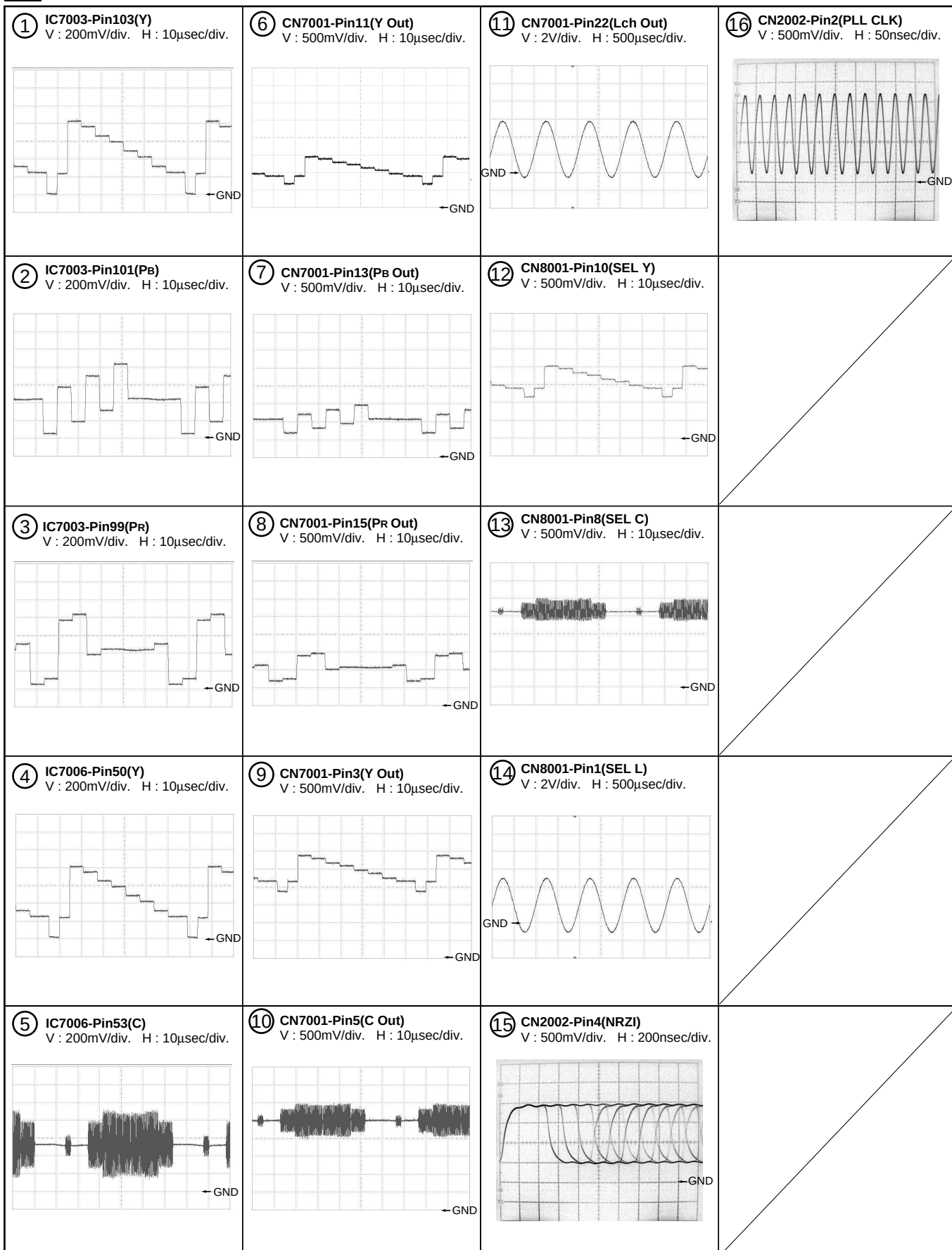


A TUMJ ASSY(2/2)**C** 3D Y/C ASSY**21** IC1312-Pin11
V : 500mV/div. H : 10 μ sec/div.**26** C1054-(+)side(ROUT)
V : 2V/div. H : 200 μ sec/div.**1** IC3001-Pin88(CVBS)
V : 500mV/div. H : 10 μ sec/div.**22** IC1351-Pin15
V : 500mV/div. H : 10 μ sec/div.**2** CN3501-Pin20(TDY)
V : 1V/div. H : 10 μ sec/div.**23** IC1351-Pin12
V : 500mV/div. H : 10 μ sec/div.**3** CN3501-Pin18(TDC)
V : 1V/div. H : 10 μ sec/div.**24** IC1351-Pin9
V : 500mV/div. H : 10 μ sec/div.**25** C1057-(+)side(LOUT)
V : 2V/div. H : 200 μ sec/div.

WAVEFORMS

Note : The encircled numbers denote measuring point in the schematic diagram.

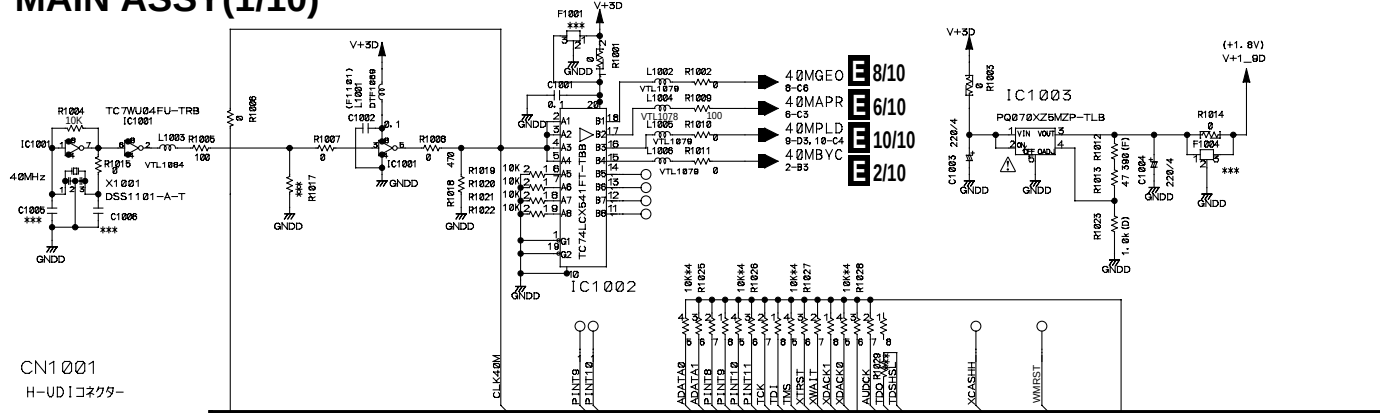
E MAIN ASSY



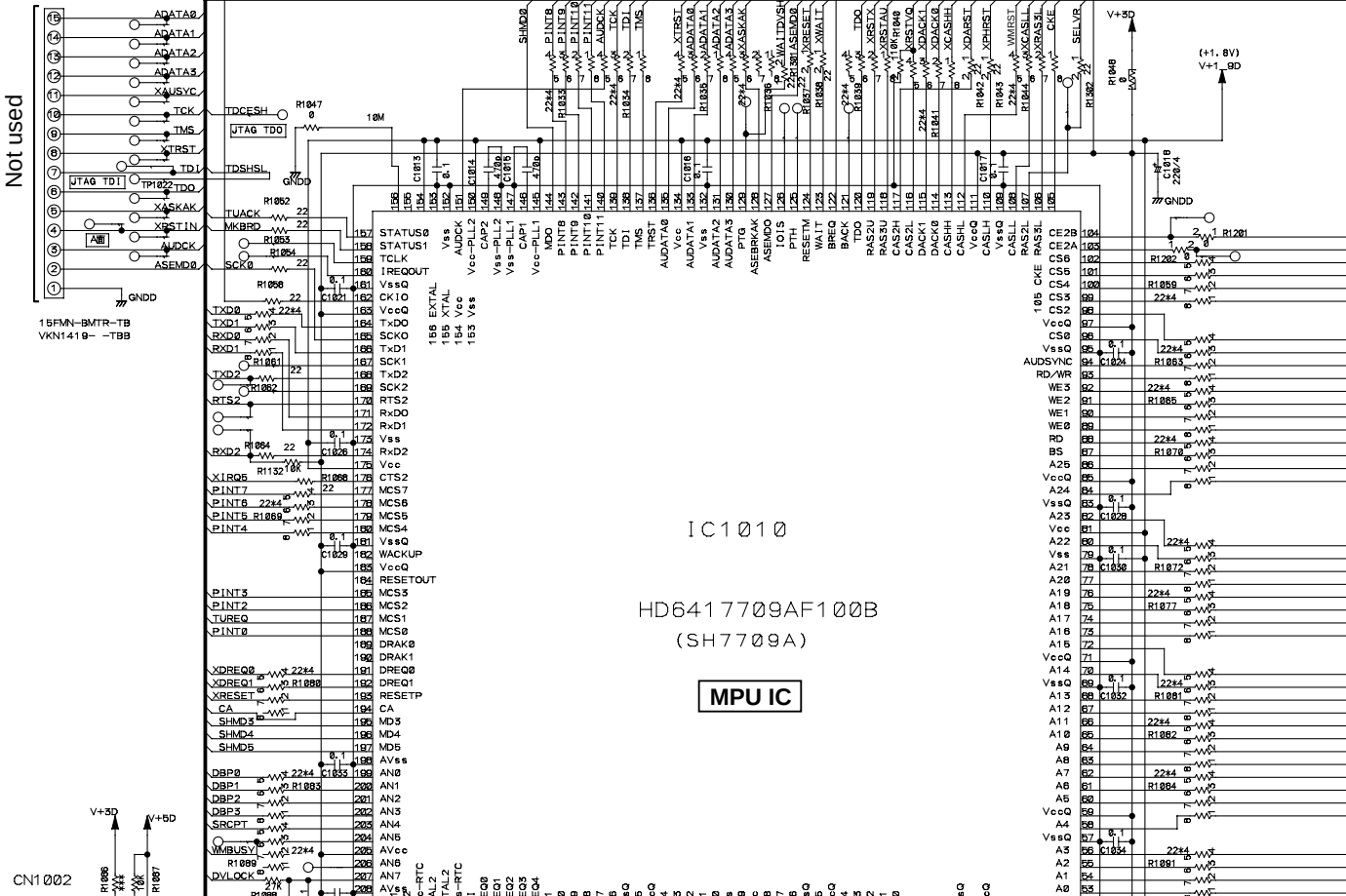
DVR-7000

3.7 MAIN ASSY(1/10)

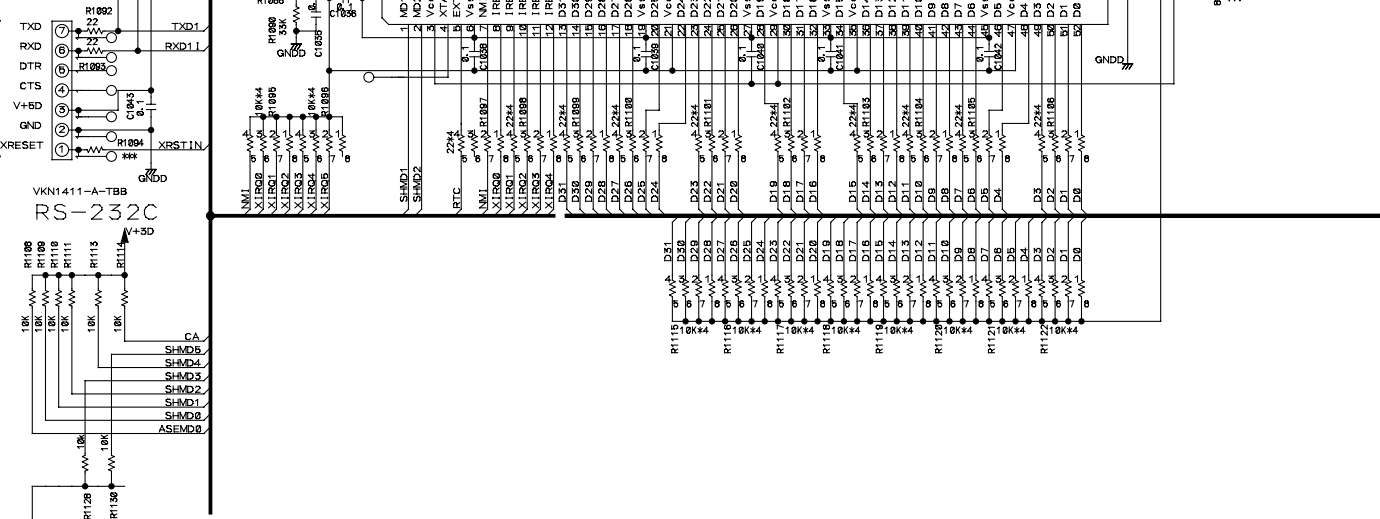
A



B

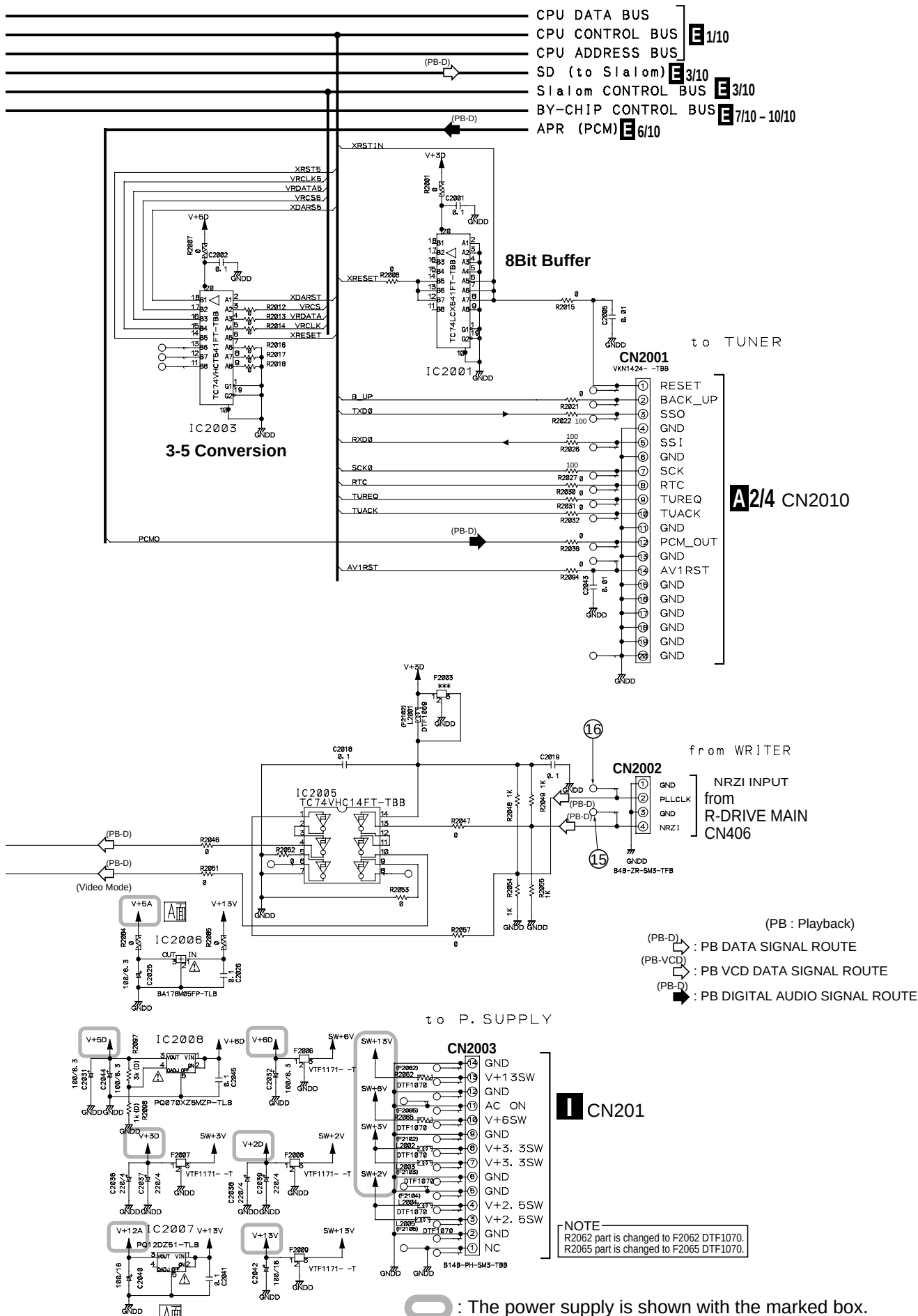


C



D



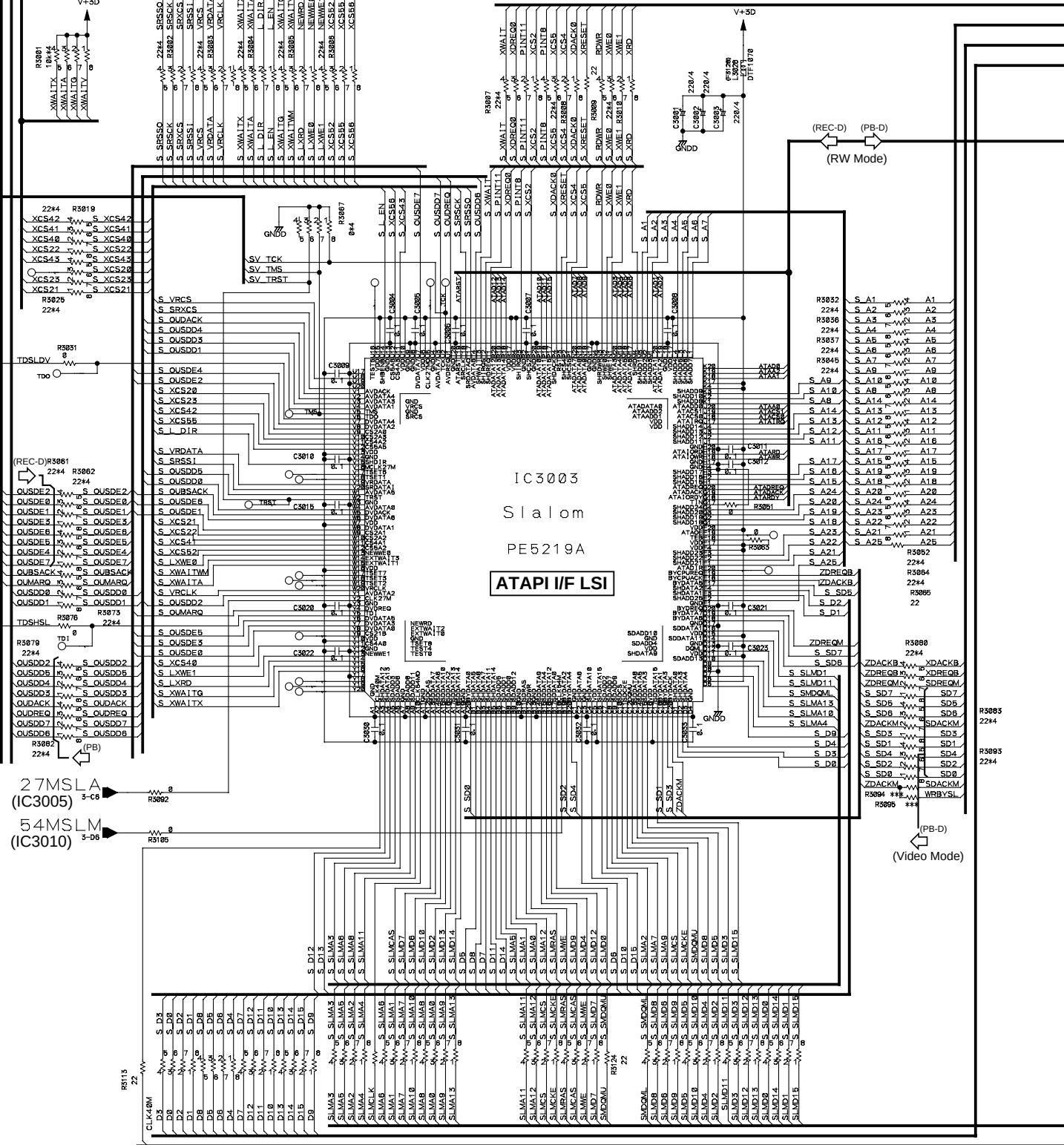


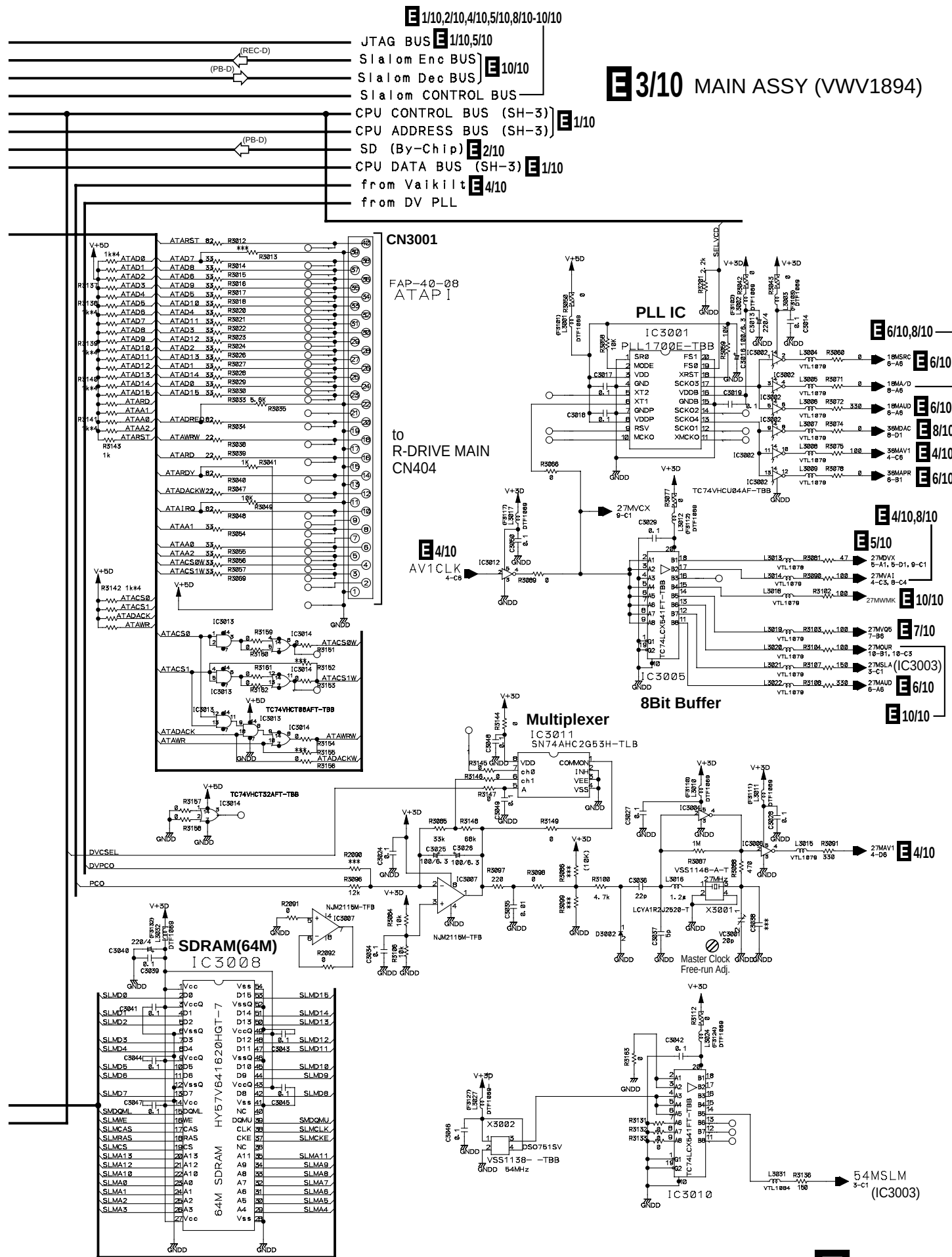
A

B

C

D





DVR-7000

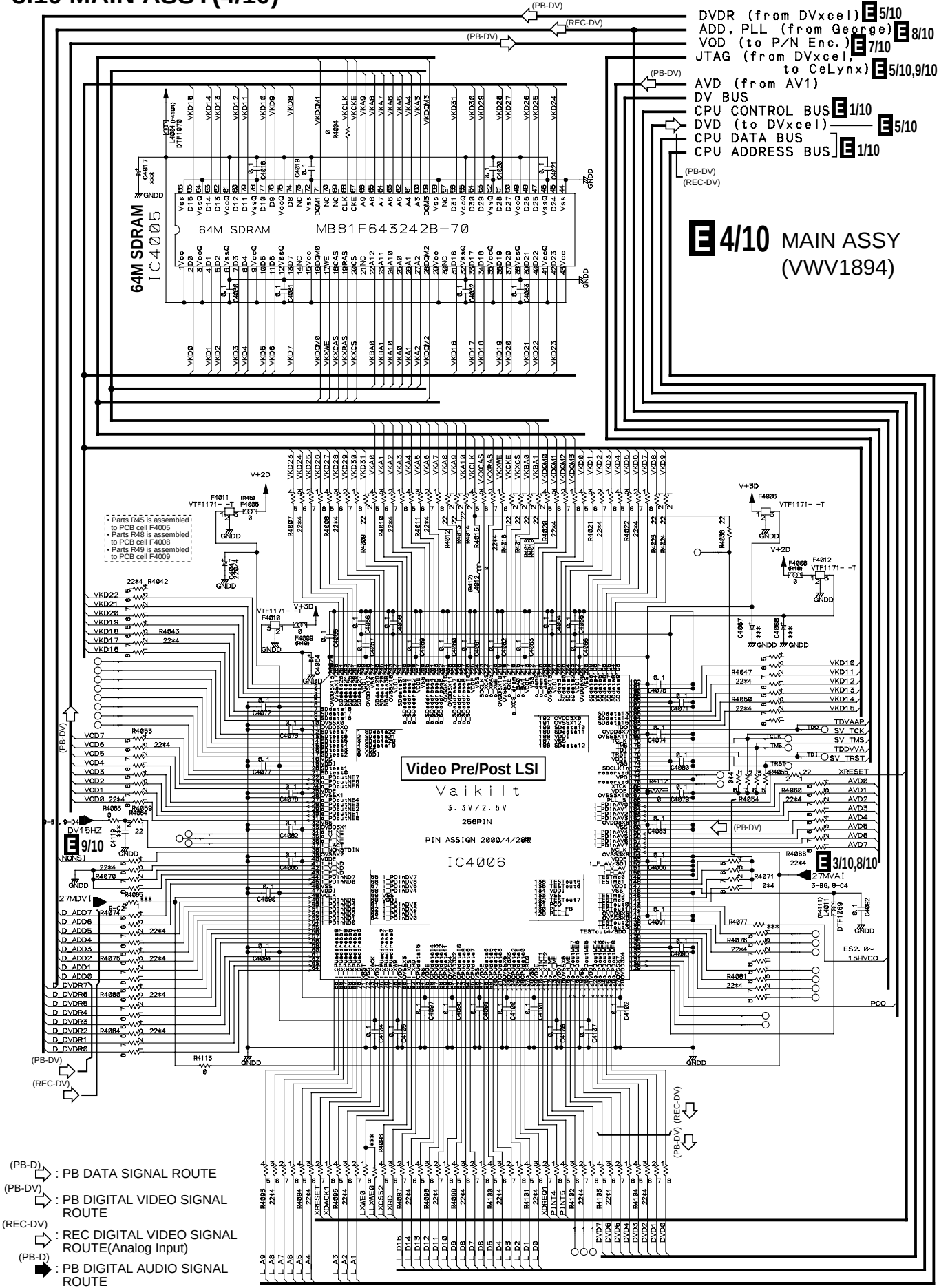
3.10 MAIN ASSY(4/10)

A

B

C

D

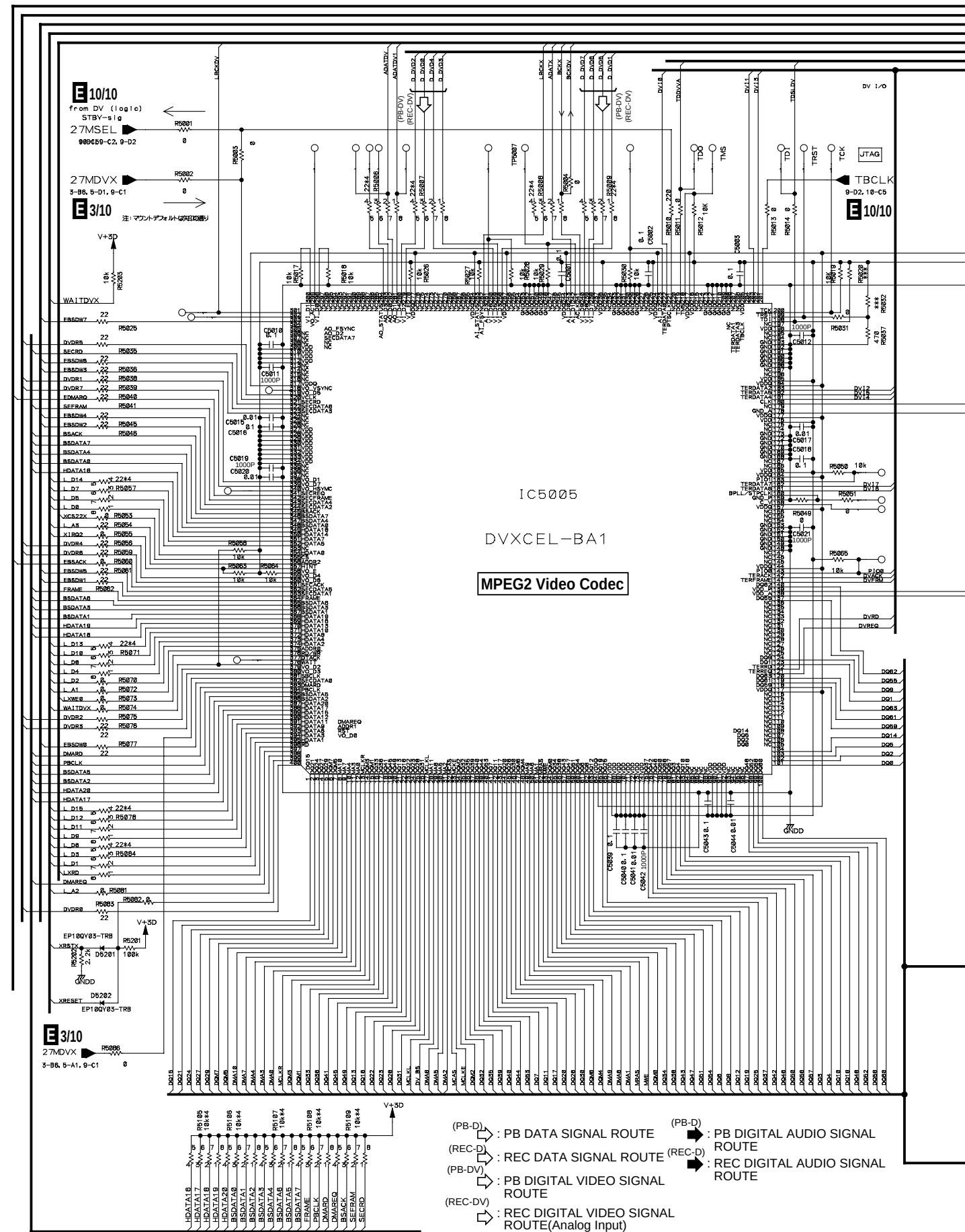


DVDR (from DVxcel) E5/10
 ADD, PLL (from George) E8/10
 VOD (to P/N Enc.) E7/10
 JTAT (from DVxcel, to CeLynx) E5/10,9/10
 AVD (from AV1)
 DV BUS
 CPU CONTROL BUS E1/10
 DVD (to DVxcel) E5/10
 CPU DATA BUS
 CPU ADDRESS BUS E1/10

E 4/10 MAIN ASSY (VWV1894)



DVR-7000
3.11 MAIN ASSY(5/10)





C



DVR-7000

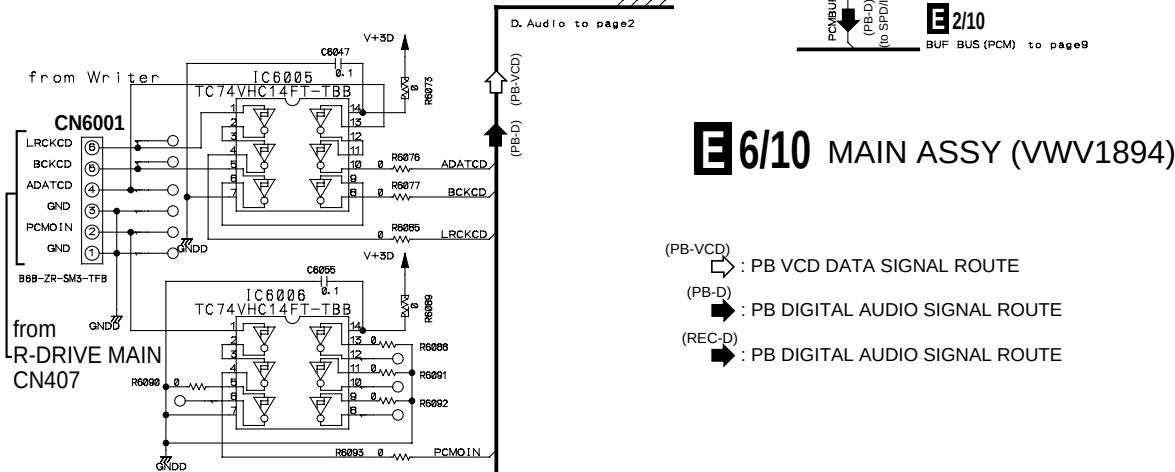
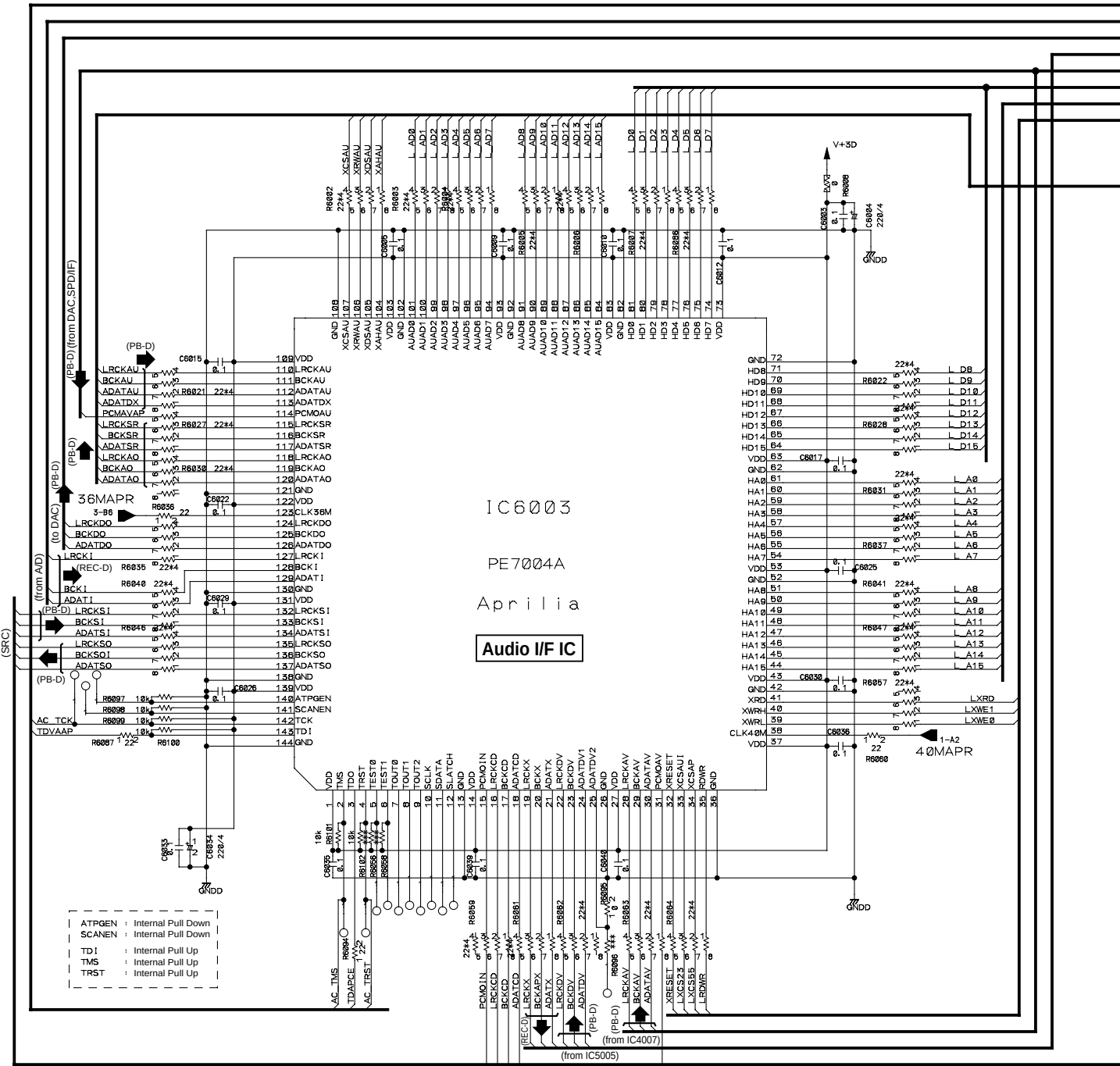
3.12 MAIN ASSY(6/10)

A

B

C

D





DVR-7000

3.13 MAIN ASSY(7/10)

7/10 MAIN ASSY (VWV1894)

SGRAM(16M)

- (PB-DV) : PB DIGITAL VIDEO SIGNAL ROUTE
- (Y) : Y VIDEO SIGNAL ROUTE
- (C) : CHROMA VIDEO SIGNAL ROUTE
- (C-Y) : COMPONENT Y SIGNAL ROUTE
- (PB) : COMPONENT Pb SIGNAL ROUTE
- (Pr) : COMPONENT Pr SIGNAL ROUTE
- ◆ : AUDIO SIGNAL ROUTE(L ch)

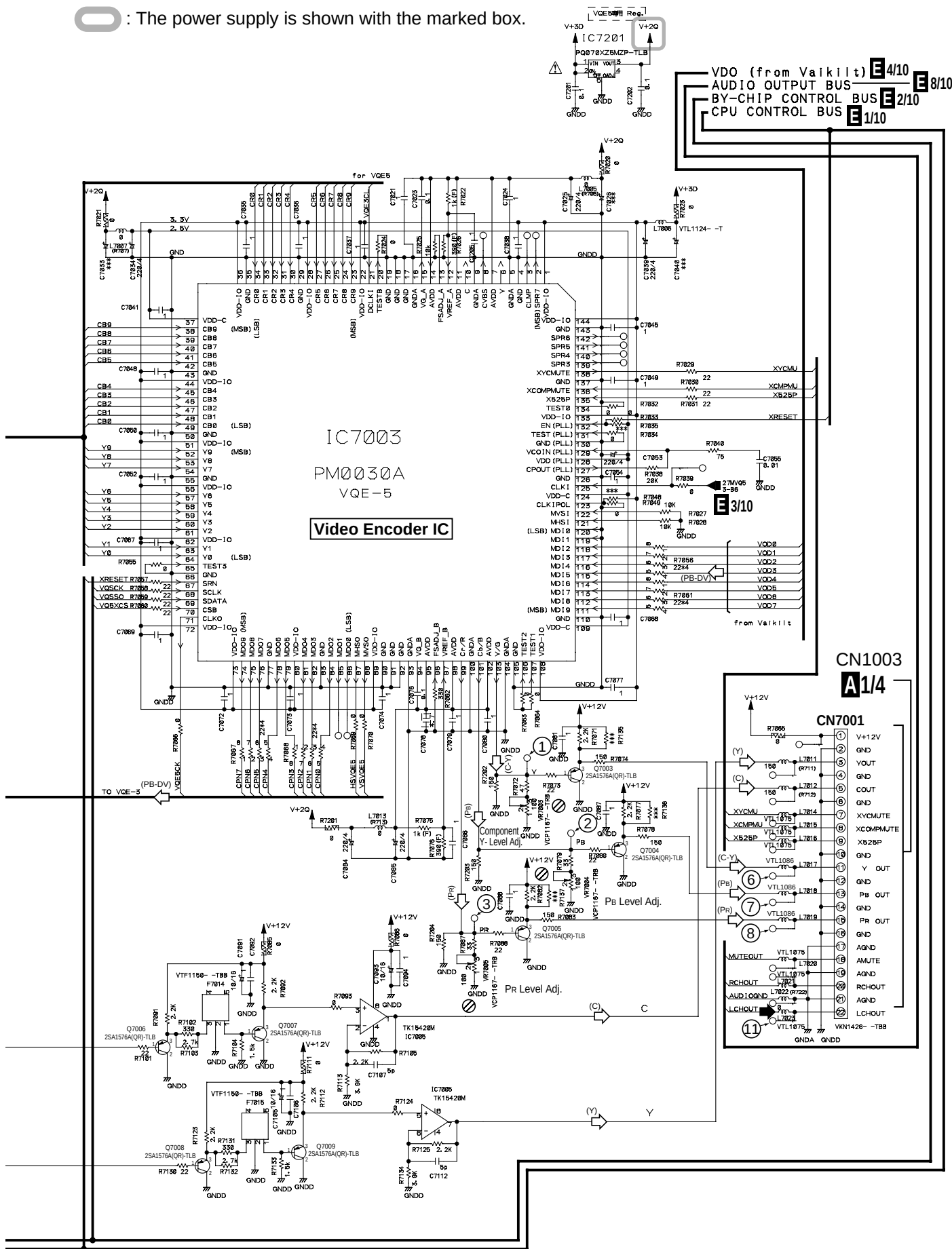
Video Encoder IC

GND A 56
CVBS 55
VDD 54
C 53

CVBS-Y
Level Adj.

C Level Adj.

 : The power supply is shown with the marked box.



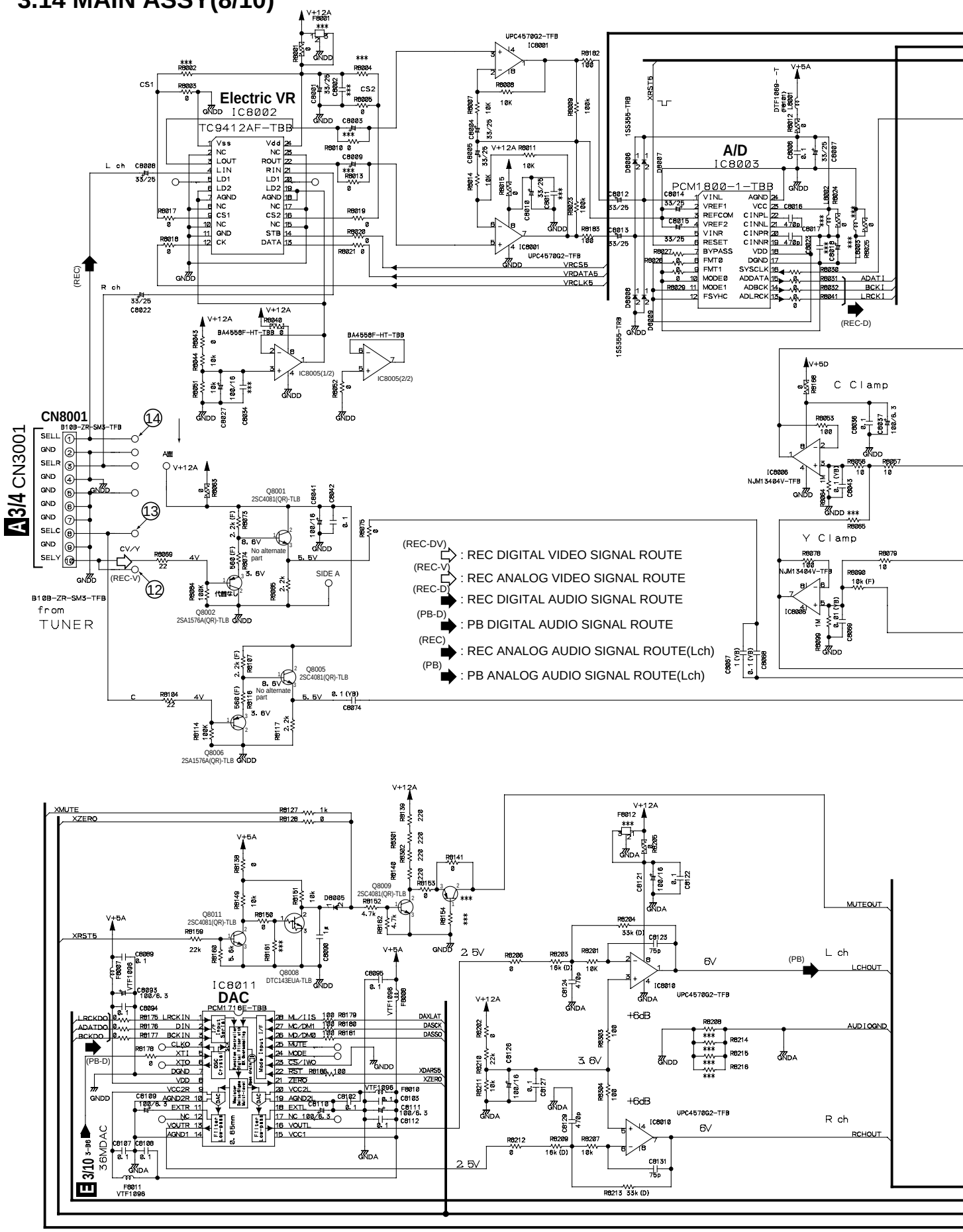
3.14 MAIN ASSY(8/10)

A

B

C

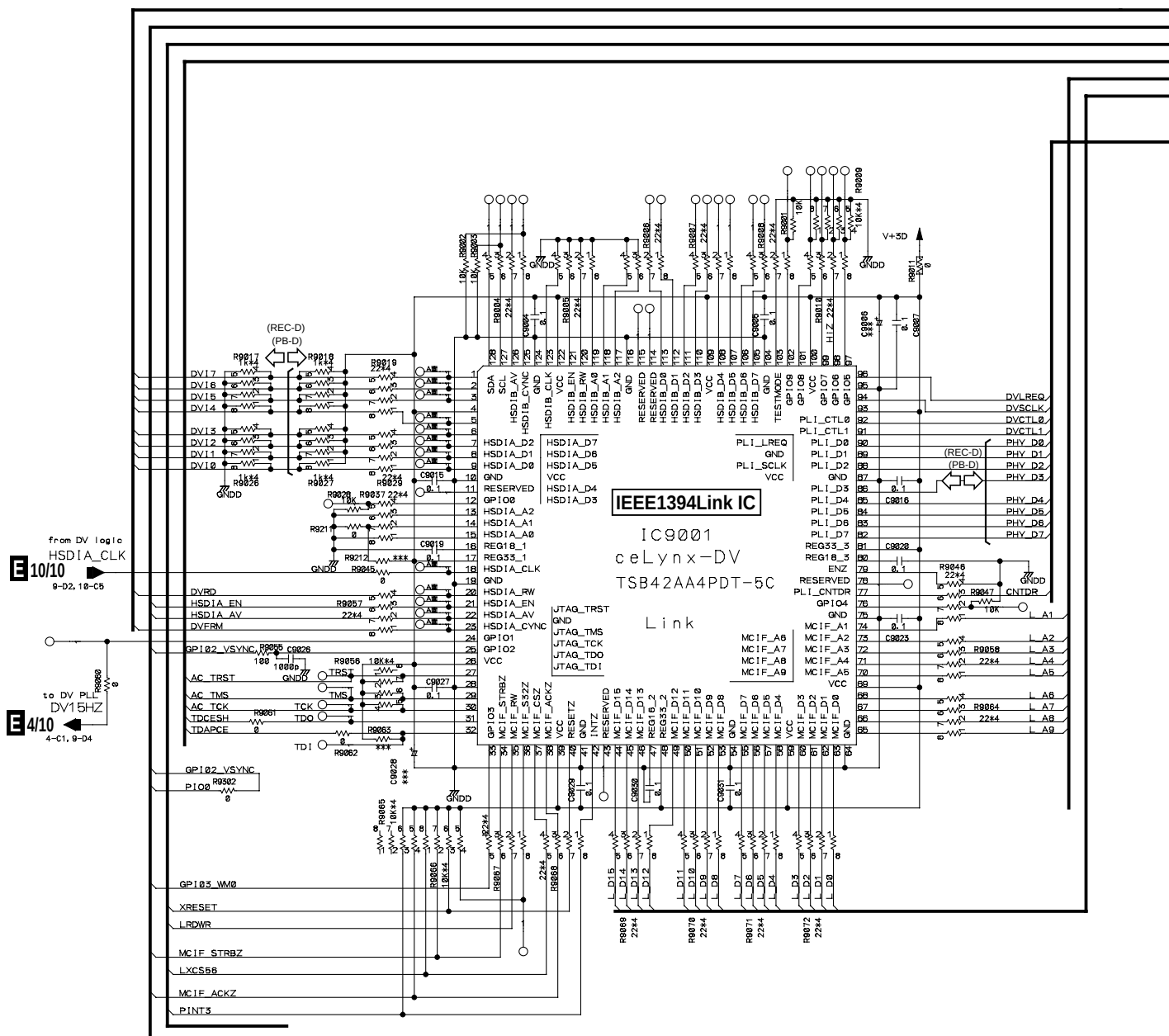
D

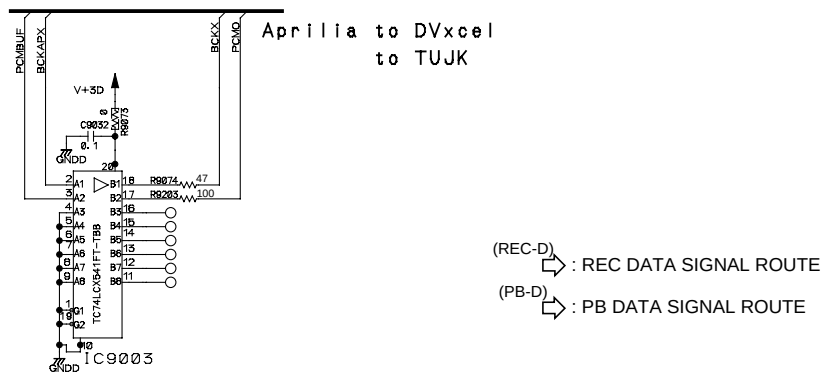
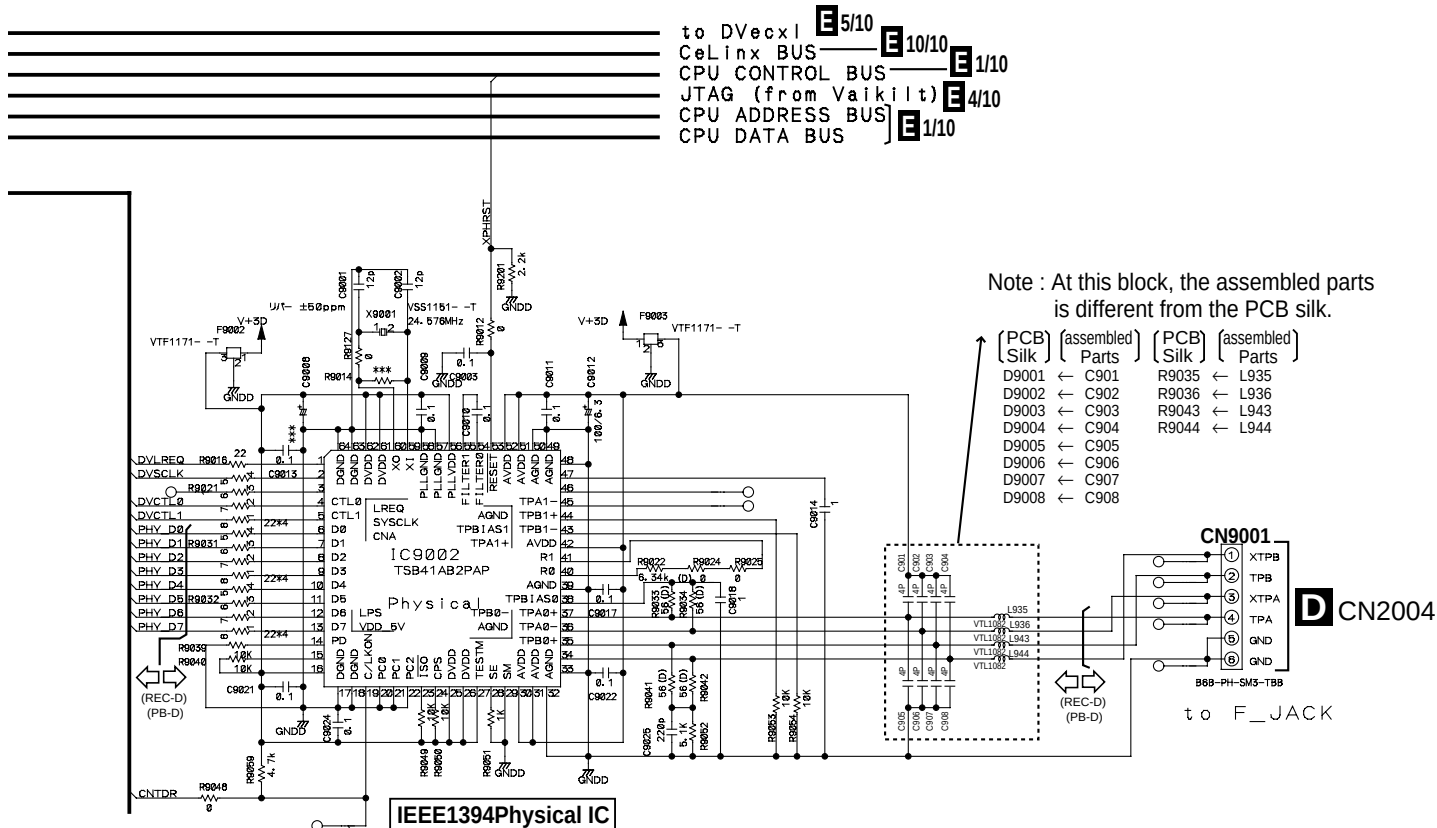




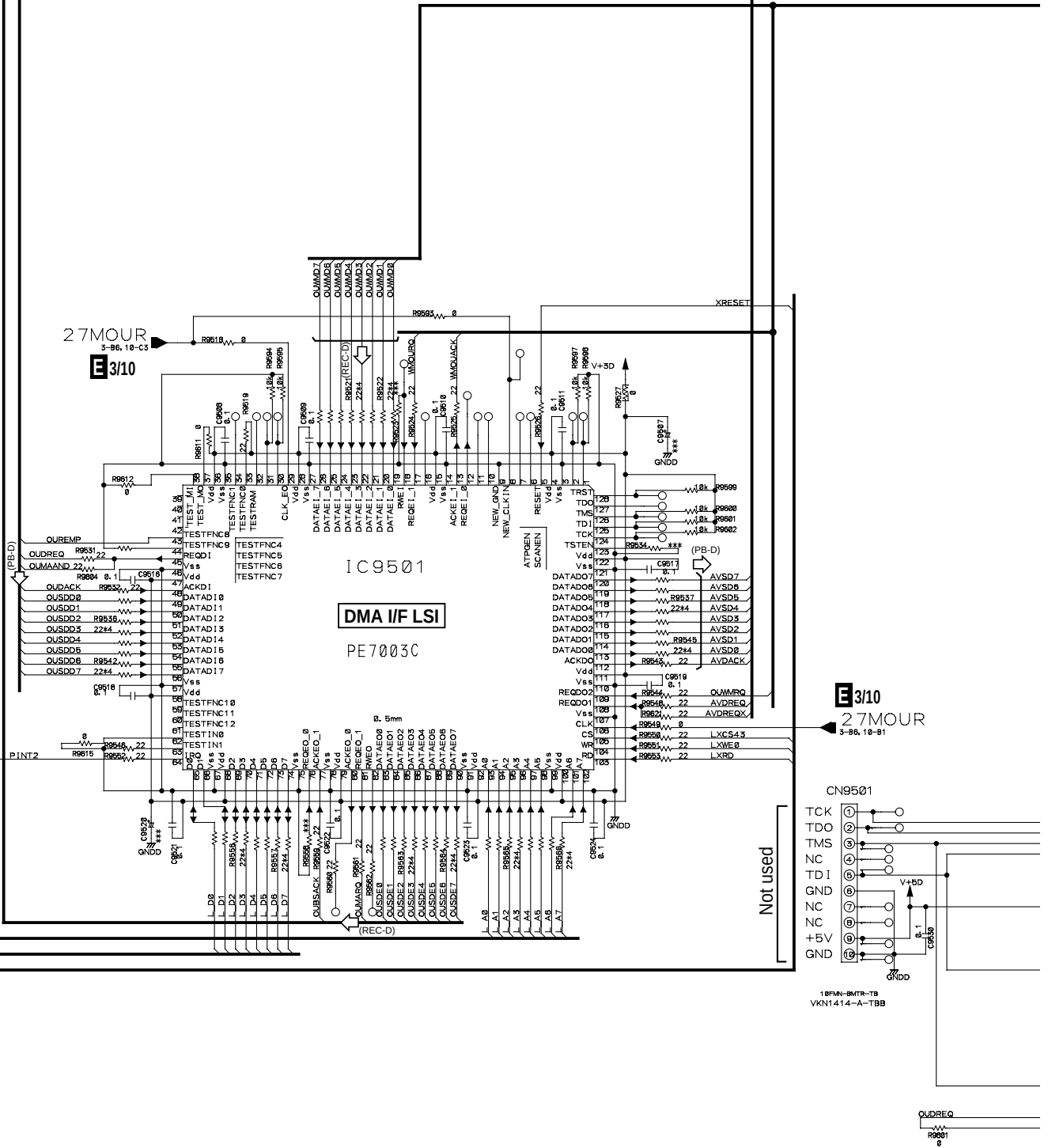
3.15 MAIN ASSY(9/10)

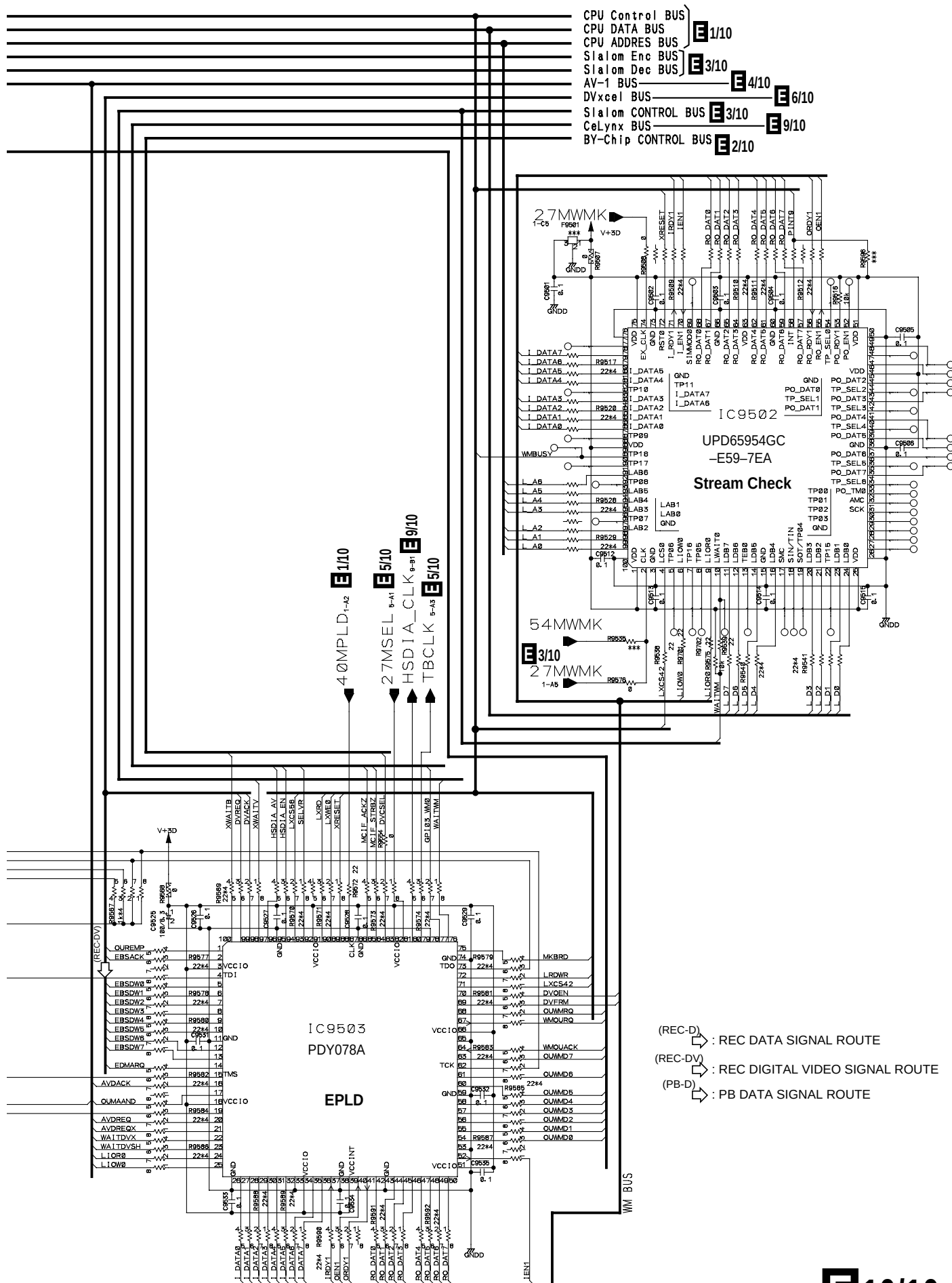
E 9/10 MAIN ASSY (VWV1894)





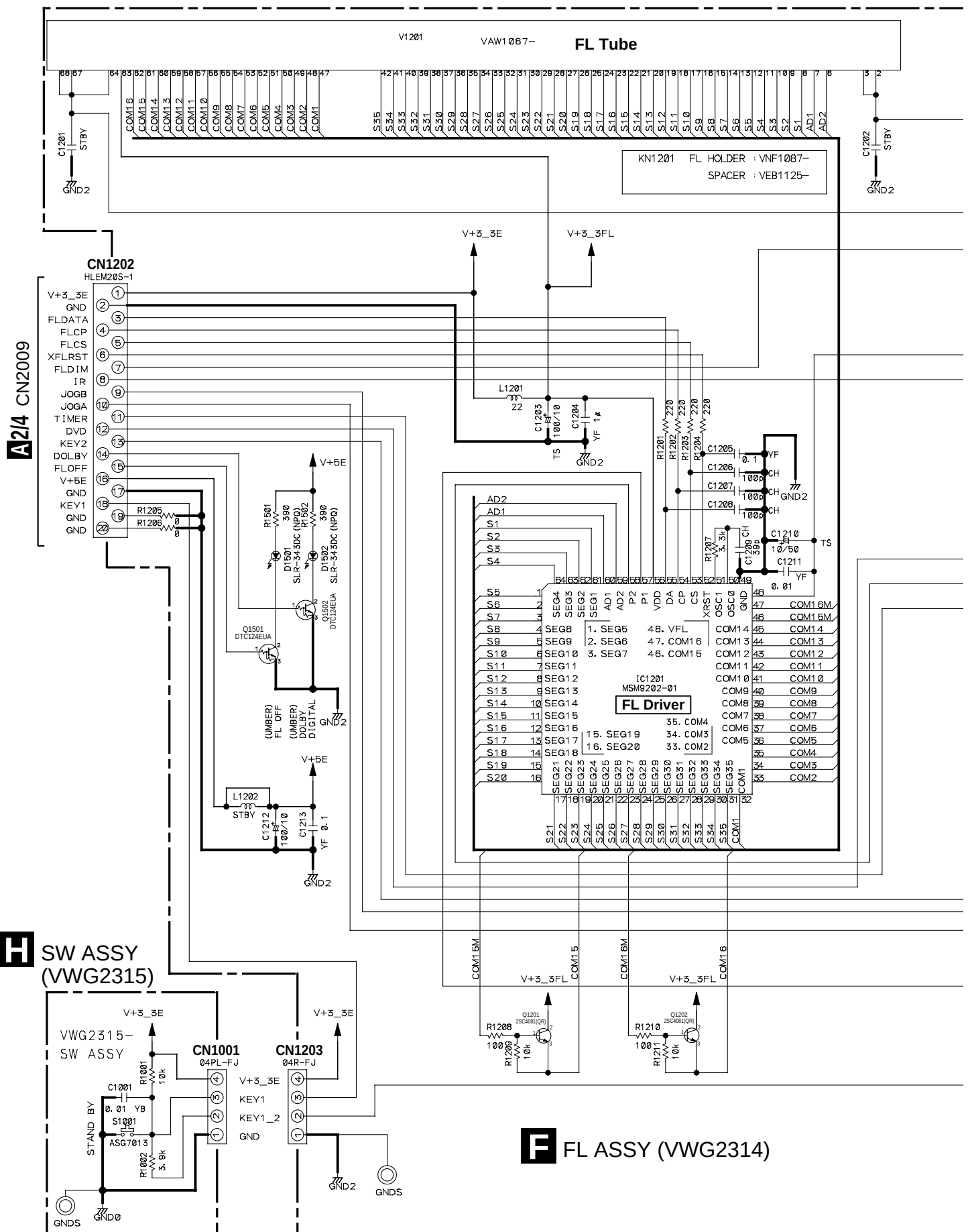
E 10/10 MAIN ASSY (VWV1894)

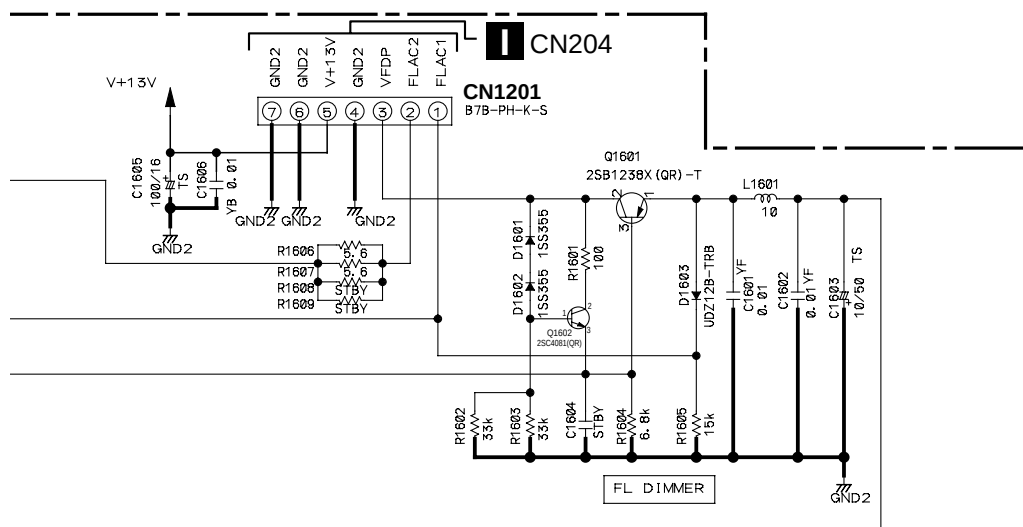




(REC-D) ➡ : REC DATA SIGNAL ROUTE
(REC-DV) ➡ : REC DIGITAL VIDEO SIGNAL ROUTE
(PB-D) ➡ : PB DATA SIGNAL ROUTE

3.17 FL, JOG and SW ASSYS



**Switches****FL ASSY**

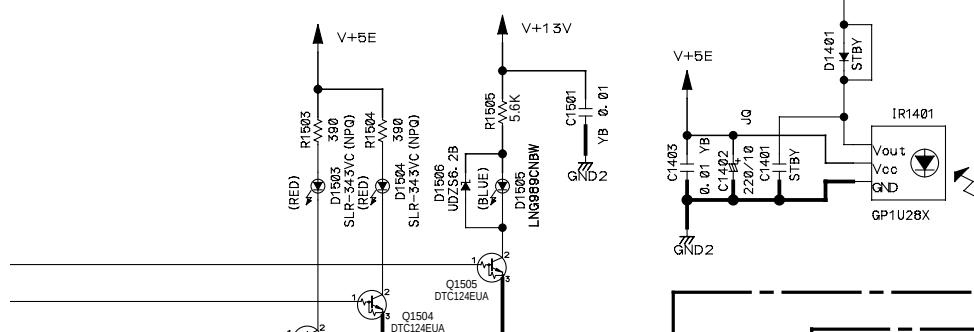
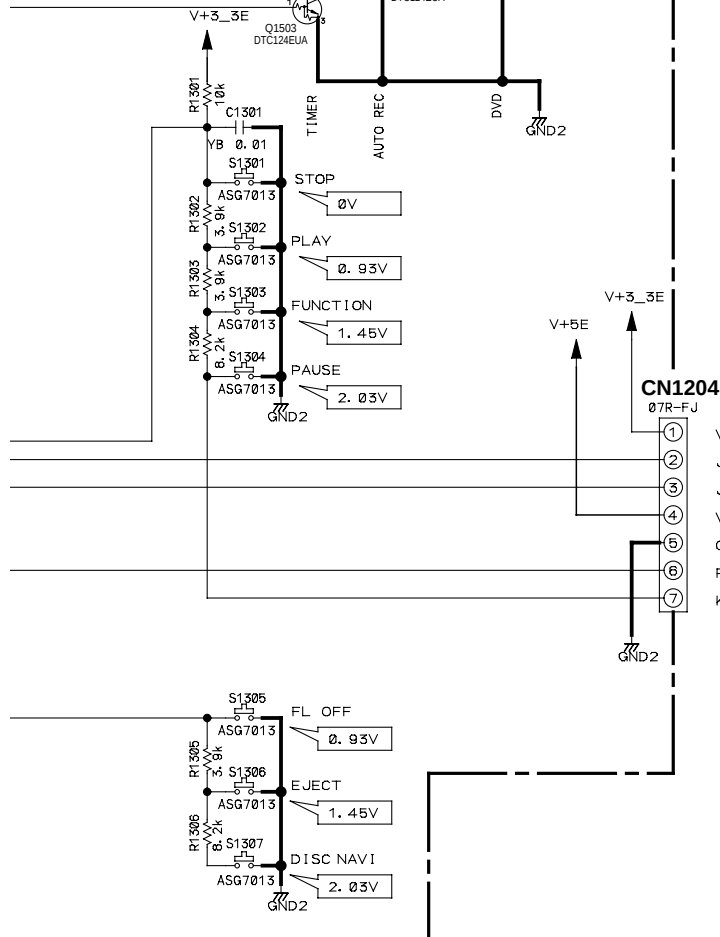
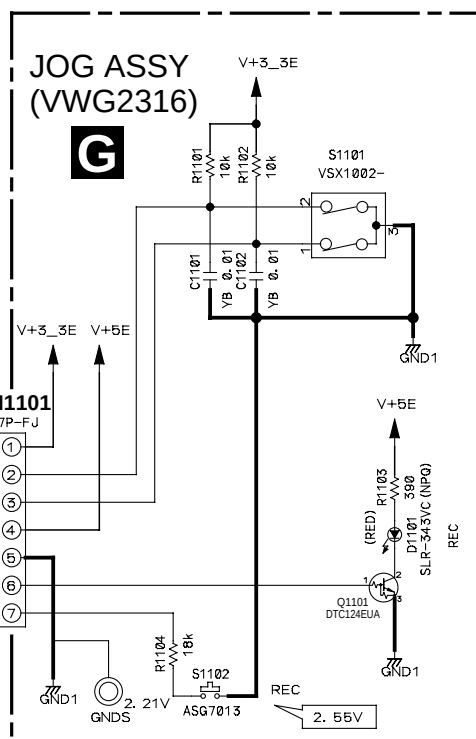
S1301 : STOP
 S1302 : PLAY
 S1303 : FUNCTION
 S1304 : PAUSE
 S1305 : FL OFF
 S1306 : EJECT
 S1307 : DISC NAVI

JOG ASSY

S1101 : SMART JOG
 S1102 : REC

SW ASSY

S1001 : STAND BY

**JOG ASSY
(VWG2316)****G**



C

D

- In case of repairing, use the described parts only to prevent an accident.
- Please write the red ✓ mark on the board when the primary section of POWER SUPPLY (SYPS) Unit is repaired.
- Please take care to keep the space, not touching other parts when replacing the parts.

4. PCB CONNECTION DIAGRAM

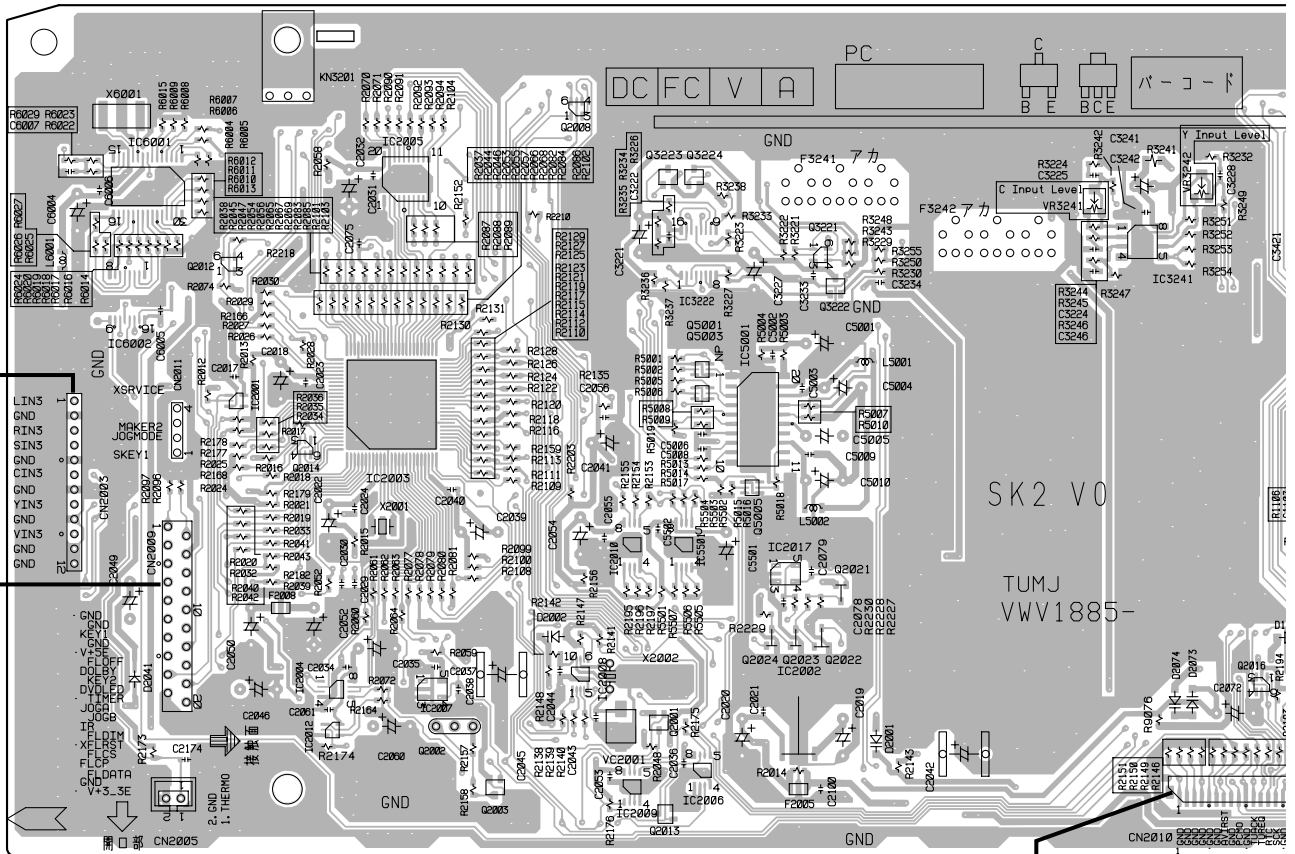
4.1 TUMJ ASSY

A

B

C

D



A TUMJ ASSY

(VNP1844-B)

E CN2001

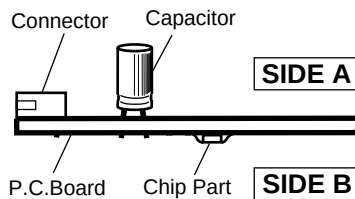
E CN8001
E CN7001

NOTE FOR PCB DIAGRAMS :

1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

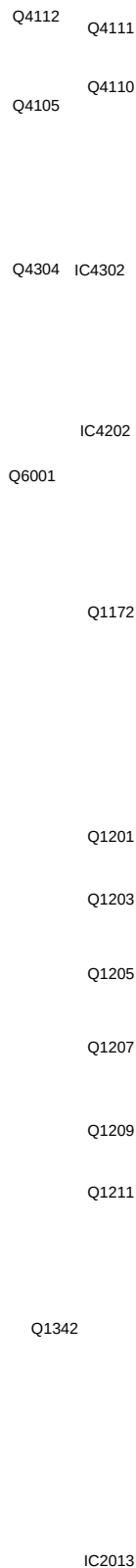
Symbol In PCB Diagrams	Symbol In Schematic Diagrams	Part Name
		Transistor
		Transistor with resistor
		Field effect transistor
		Resistor array
		3-terminal regulator

3. The parts mounted on this PCB include all necessary parts for several destinations.
- For further information for respective destinations, be sure to check with the schematic diagram.
4. View point of PCB diagrams.



FAN MOTOR
FAN MOTOR

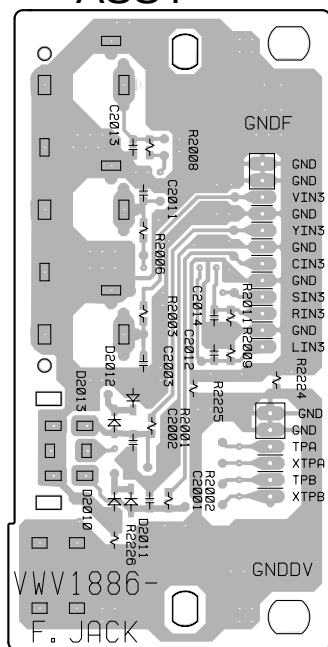
I CN202





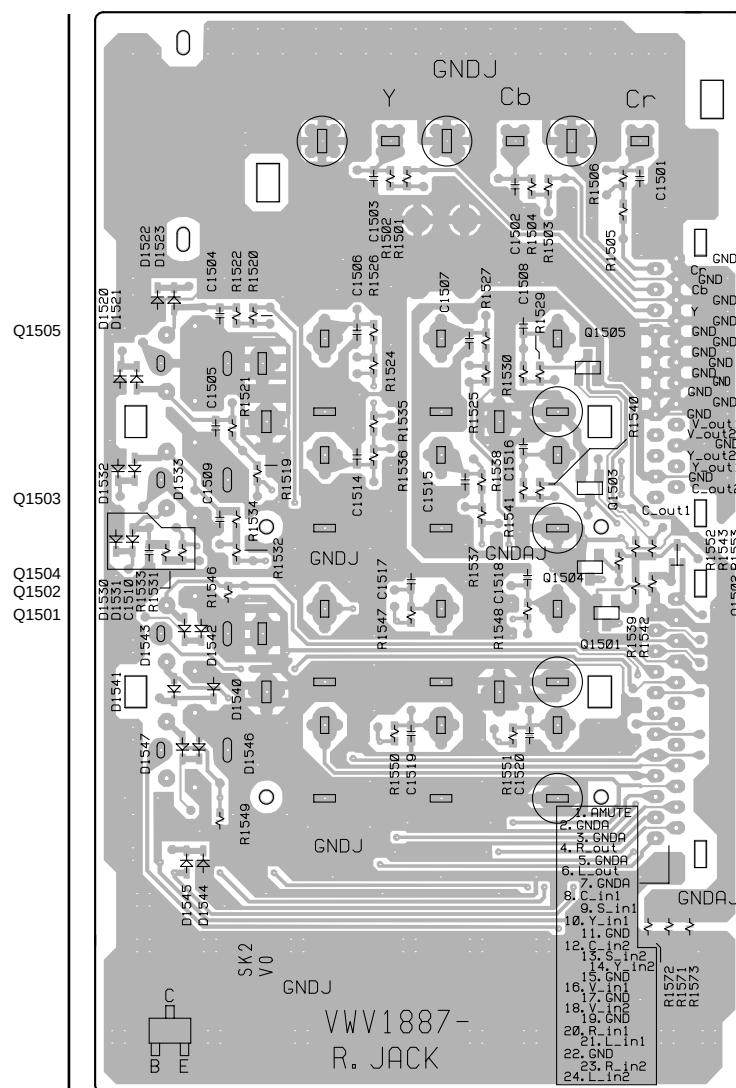
A TUMJ ASSY

FRONT JACK ASSY



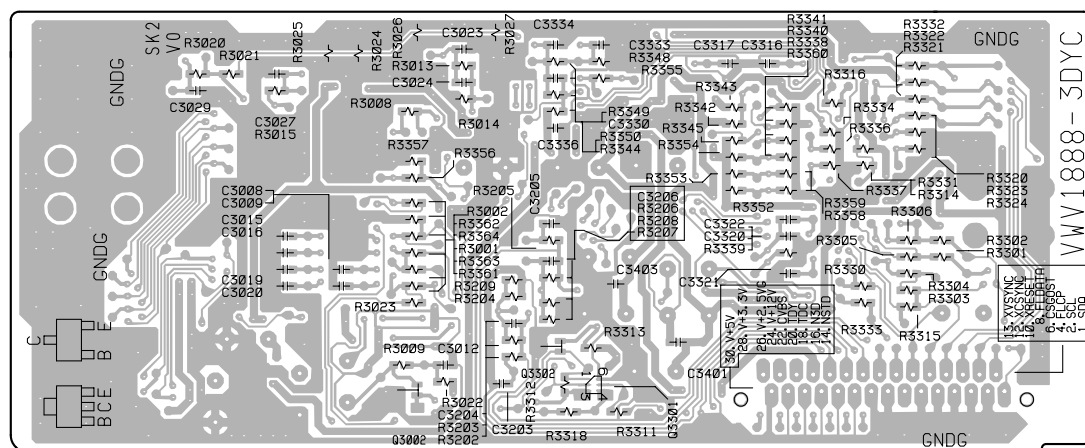
(VNP1844-B)

B REAR JACK ASSY



(VNP1844-B)

C 3D Y/C ASSY



(VNP1844-B)

Q3002

Q3301

SIDE B

B C D

4.3 MAIN ASSY

E MAIN ASSY

A CN3001

A CN2010

A CN1003

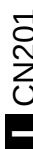
D CN2004

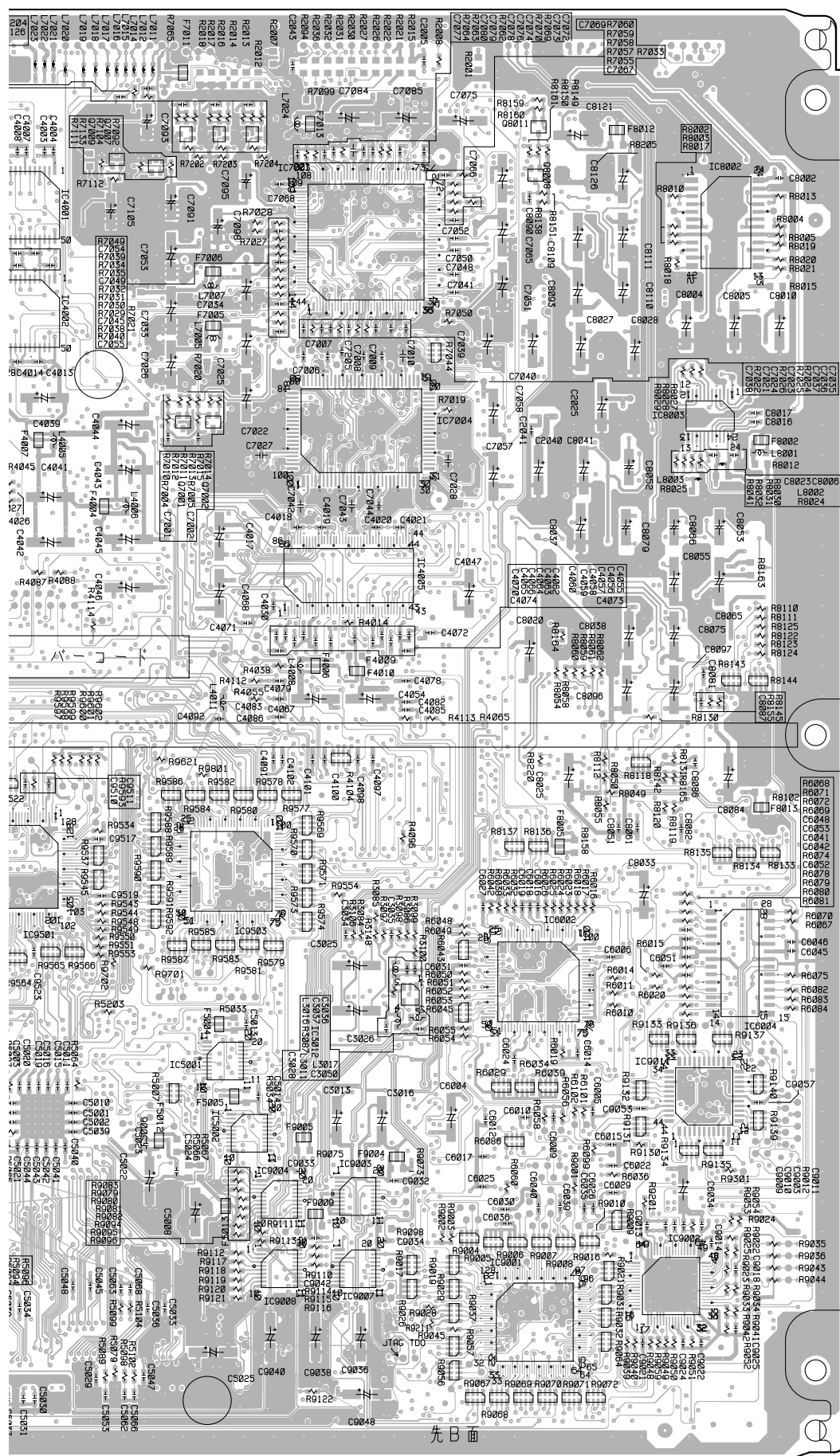
SIDE A

(VNP1846-C)

MAIN 後A面 耐フリ

VNP1846

ABCD

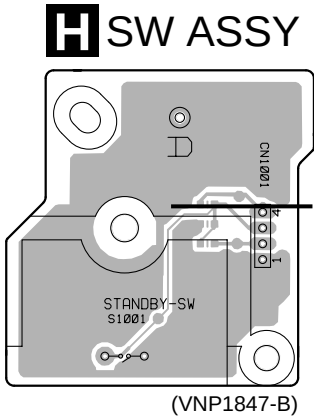


SIDE B

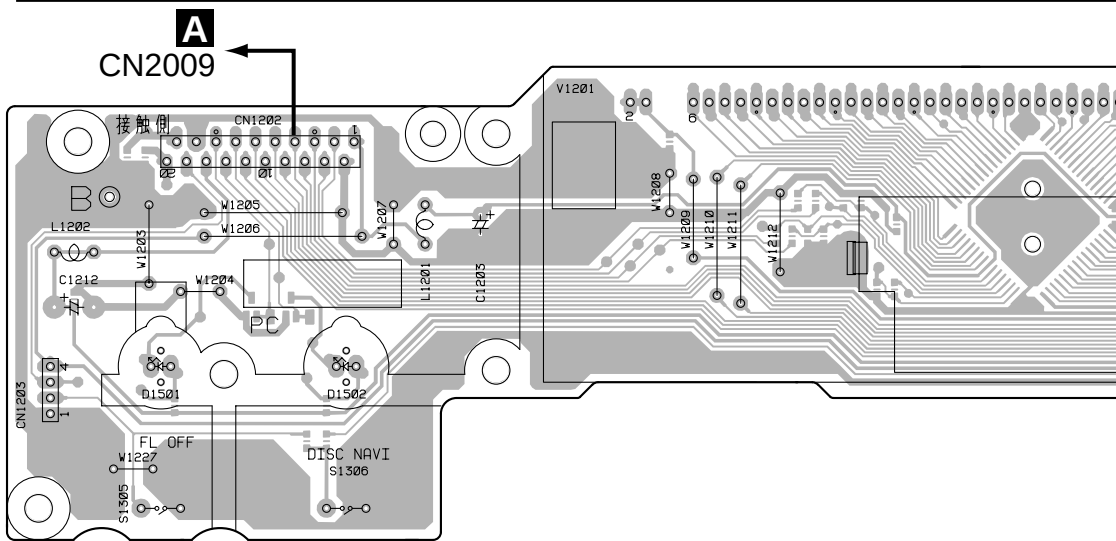
(VNP1846-C)

4.4 FL, JOG AND SW ASSYS

A



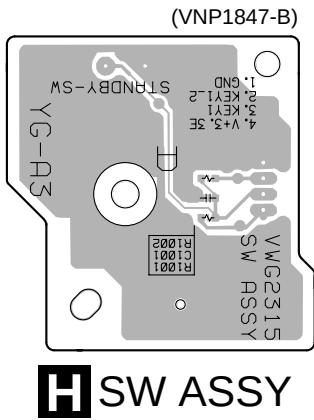
B



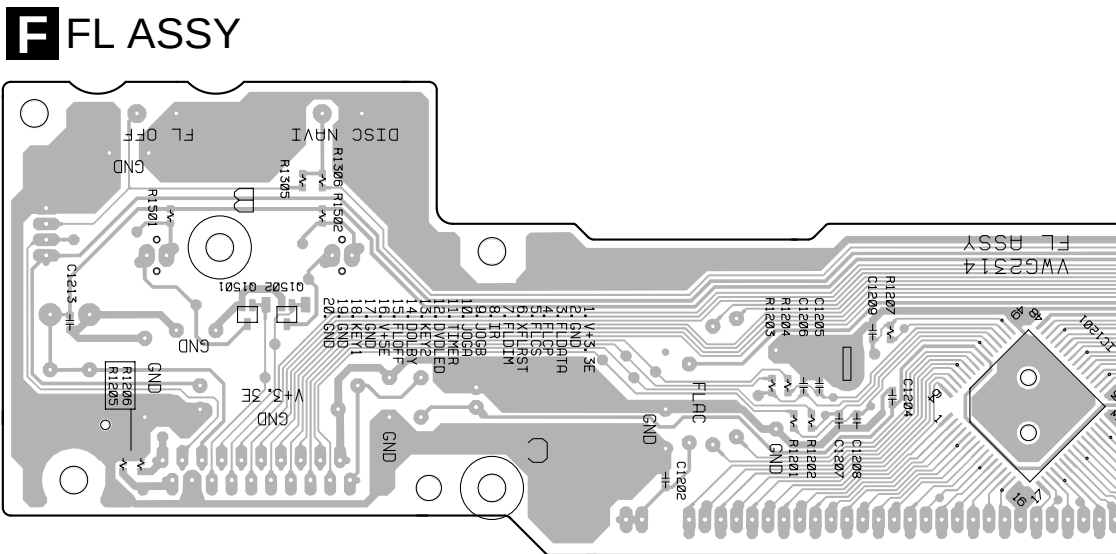
SIDE A

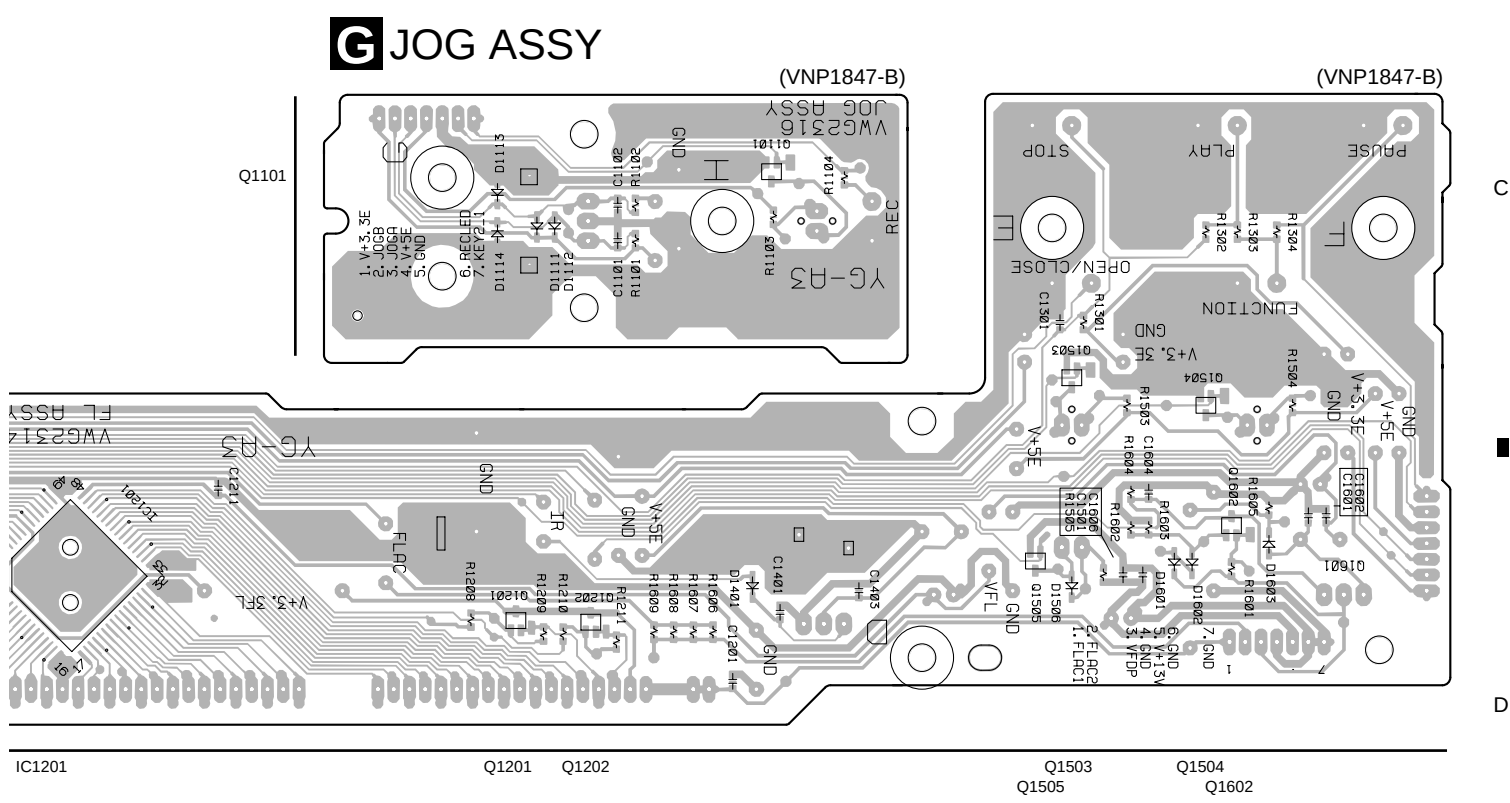
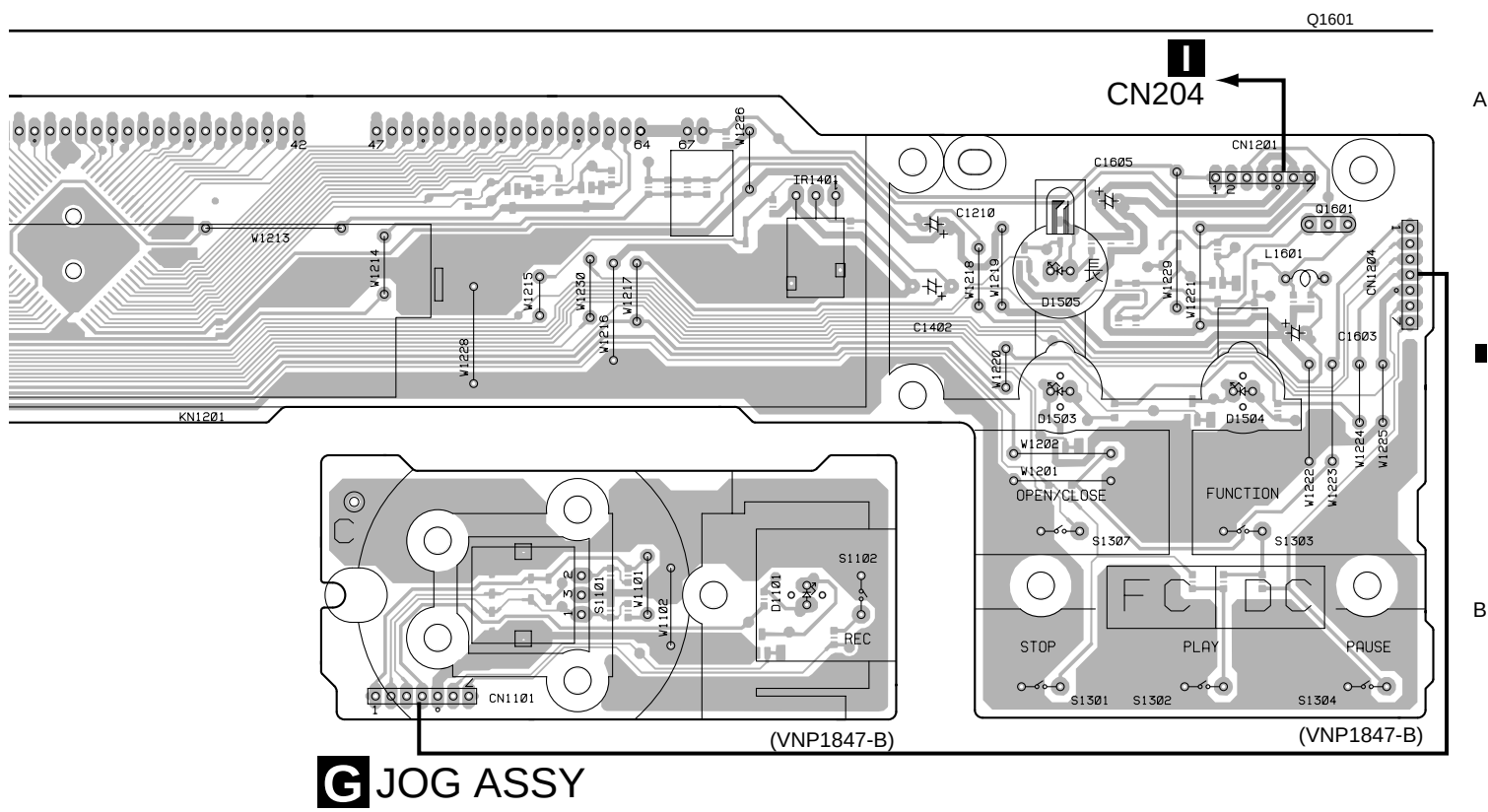
SIDE B

C



D





5. PCB PARTS LIST

NOTES: ●Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.

●The Δ mark found on some component parts indicates the importance of the safety factor of the part.

Therefore, when replacing, be sure to use parts of identical designation.

●When ordering resistors, first convert resistance values into code form as shown in the following examples.

Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).

560 Ω $\rightarrow$ 56×10^1 $\rightarrow$ 561 RD1/4PU $\boxed{5} \boxed{6} \boxed{1} J$
 47k Ω $\rightarrow$ 47×10^3 $\rightarrow$ 473 RD1/4PU $\boxed{4} \boxed{7} \boxed{3} J$
 0.5 Ω $\rightarrow$ R50 RN2H $\boxed{R} \boxed{5} \boxed{0} K$
 1 Ω $\rightarrow$ 1R0 RS1P $\boxed{1} \boxed{R} \boxed{0} K$

Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62k Ω $\rightarrow$ 562×10^1 $\rightarrow$ 5621 RN1/4PC $\boxed{5} \boxed{6} \boxed{2} \boxed{1} F$

Mark	No.	Description	Part No.
------	-----	-------------	----------

LIST OF ASSEMBLIES

	TUJB ASSY	VWM2103
	└ TUMJ ASSY	VWV1885
	└ REAR JACK ASSY	VWV1887
	└ 3D Y/C ASSY	VWV1888
	└ FRONT JACK ASSY	VWV1886

	MAIN ASSY	VWV1894
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	FLKB ASSY	VWM2105
	└ FL ASSY	VWG2314
	└ JOG ASSY	VWG2316
	└ SW ASSY	VWG2315

Δ	POWER SUPPLY ASSY	VWR1347
----------	-------------------	---------

A TUMJ ASSY SEMICONDUCTORS

	IC2002	BA033FP
	IC2013	BA10393F
	IC4402	BA4558F-HT
	IC1102	BA7046F
	IC1351	BA7665FS

	IC2010,IC5501	BR24E16FV
	IC3222,IC4201	BU4052BCFV
	IC4601	CXA2094Q
	IC5001	LC7454M
	IC1002	MM1114XF

Δ	IC1003,IC1004,IC1171	MM1118XF
	IC2003	PE5275B9
	IC2011	PQ12RF11
	IC2017	PST9120N
	IC2007	PST9130N

	IC2008	RV5C386A
	IC1421,IC2001,IC2012	SN74AHC1G08HDCK
	IC2006	SN74AHC2G126HDCT
	IC2004	SN74AHC2GU04HDCT
	IC1001,IC1301	SN74LV4053APW

	IC2009	TC4W53FU
	IC2005	TC74VHCT541AFT
	IC1101	TC7WH123FU
	IC3241	TK15420M
	IC1311	TK15452V

	IC1312	TK15453V
	IC4202,IC4302	UPC4570G2
	Q1102,Q1103,Q1106,Q1205	2SA1576A

Mark	No.	Description	Part No.
------	-----	-------------	----------

	Q1207,Q1209,Q4110	2SA1576A
	Q2006,Q4411	2SB1132
	Q2002	2SB1237X
	Q1311,Q1411,Q2023,Q3222,Q4102	2SC4081
	Q2004,Q2007,	

	Q2009,Q2010,Q2022	2SD2114K
	Q1104	2SK210
	Q1105,Q1108,Q2001,Q2021	DTA124EUA
	Q1172,Q1333,Q1341,Q2013,Q2024	DTC124EUA
	Q3223	DTC124EUA

	Q2003,Q2005,Q4412	DTC143EUA
	Q1101,Q1113,Q1221-Q1232,Q4111	HN1A01FU
	Q3221,Q4103,Q4104	HN1B01FU
	Q1112,Q1114,Q1115,Q2008	HN1K03FU
	Q2012,Q2015,Q4601	HN1K03FU

	Q4201,Q5001,Q5003,Q5005	RN1903
	Q2014	RN2903
	D2003	1SR154-400
	D2001,D2002,D2073,D2074	EP10QY03
	D1101,D1401,D2021-D2023,D2041	MA111

	D4302,D4501	MA111
	D4101	UDZ33B
	D4301	UDZS9.1B

COILS AND FILTERS

	L1401,L1412,L5001,L5002	LCTA100J2520
	L1101	LCTA330J2520
	F1202,F1204,F1206,F3241,F3242	VTF1166
	F1201,F1203,F1205	VTF1167
	F1821,F1831,F2007-F2009	VTF1170

	L4101,L4102	VTL1096
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CAPACITORS

	C1120,C2043,C2281-C2286	CCSRCH100D50
	C1335-C1337,C2029,C2030	CCSRCH101J50
	C4150,C4151	CCSRCH101J50
	C1003,C1010,C1035,C1115	CCSRCH102J50
	C1108,C1124	CCSRCH120J50

	C4202,C4216,C4303,C4333,C9402	CCSRCH220J50
	C1113	CCSRCH221J50
	C1107	CCSRCH390J50
	C4502	CCSRCH470J50
	C4325,C4334	CCSRCH681J50

	C5007	CCSRCH821J50
	C1351,C5005	CEANP2R2M50
	C4322,C4602,C4606,C4607,C4610	CEANP4R7M50

Mark	No.	Description	Part No.
	C4615		CEANP4R7M50
	C2015,C4108,C4111,C4118,C4132		CEAT100M50
	C4205-C4207,C4221-C4223,C4320		CEAT100M50
	C4331,C4616		CEAT100M50
	C1001,C1014,C1024,C1112		CEAT101M10
	C1117,C1118,C1175,C1201,C1204		CEAT101M10
	C1207,C1301,C1311,C1317,C1354		CEAT101M10
	C1401,C1402,C1821,C1831,C2009		CEAT101M10
	C2018-C2020,C2022,C2032,C2035		CEAT101M10
	C2041,C2049,C2054,C2057,C2058		CEAT101M10
	C2060,C2062,C2072,C4103,C4106		CEAT101M10
	C4115,C4116,C4120,C4410,C4412		CEAT101M10
	C4432,C5004,C5010,C5501		CEAT101M10
	C1007,C1101,C1103,C1106,C1804		CEAT101M16
	C1811,C1812,C2006,C2007,C3221		CEAT101M16
	C3227,C3241,C4215,C4301,C4305		CEAT101M16
	C4307,C4310,C4403,C4431,C4433		CEAT101M16
	C2004,C2027		CEAT101M25
	C1320		CEAT102M6R3
	C1005,C1009,C1012,C1013		CEAT1R0M50
	C1032,C1033,C1171,C4608,C4619		CEAT1R0M50
	C1356,C1358		CEAT220M25
	C1315,C1325,C1326,C1414		CEAT221M6R3
	C5001		CEAT2R2M50
	C1054,C1057,C1312,C1313,C1327		CEAT470M16
	C1415		CEAT470M16
	C2067		CEAT471M16
	C1322,C1324,C1355,C1357,C1832		CEAT471M6R3
	C4609,C4612		CEAT4R7M50
	C4105,C4107,C4114,C4121		CKSRYB102K50
	C1006,C1016,C1023,C1176,C1412		CKSRYB103K50
	C2016,C3225,C3228,C4110,C4117		CKSRYB103K50
	C4319,C4330		CKSRYB103K50
	C1004,C1011,C1034,C1105,C1318		CKSRYB104K16
	C1352,C1359,C3224,C3246		CKSRYB104K16
	C1319,C1323		CKSRYB105K6R3
	C4618		CKSRYB123K50
	C4605		CKSRYB272K50
	C4318,C4329		CKSRYB472K50
	C4604		CKSRYB473K25
	C4617		CKSRYB562K50
	C1002,C1008,C1015,C1025,C1102		CKSRYF104Z25
	C1104,C1109-C1111,C1116,C1119		CKSRYF104Z25
	C1121,C1122,C1125,C1126		CKSRYF104Z25
	C1173,C1174,C1177,C1202,C1203		CKSRYF104Z25
	C1205,C1206,C1208,C1209,C1221		CKSRYF104Z25
	C1223,C1224,C1226,C1227		CKSRYF104Z25
	C1229,C1230,C1232,C1233		CKSRYF104Z25
	C1235,C1236,C1238,C1302,C1403		CKSRYF104Z25
	C1421,C1803,C1822,C1833,C2005		CKSRYF104Z25
	C2008,C2010,C2017,C2021		CKSRYF104Z25
	C2023,C2024,C2028,C2031		CKSRYF104Z25
	C2033,C2034,C2036-C2038,C2040		CKSRYF104Z25
	C2044,C2047,C2048,C2051,C2053		CKSRYF104Z25
	C2055,C2061,C2063-C2066		CKSRYF104Z25
	C2068-C2071,C2073,C2078-C2080		CKSRYF104Z25
	C3222,C3233,C3234,C3242,C4104		CKSRYF104Z25
	C4112,C4119,C4131,C4201,C4203		CKSRYF104Z25
	C4213,C4214,C4304,C4306,C4309		CKSRYF104Z25
	C4311,C4409,C4411,C4425		CKSRYF104Z25
	C4429,C4430,C4501,C4611,C5003		CKSRYF104Z25
	C5009,C5502		CKSRYF104Z25

Mark	No.	Description	Part No.
	C1114,C1310,C1314,C1316,C1321		CKSRYF105Z10
	C1328,C1353,C1360,C1413,C2059		CKSRYF105Z10
	C2077		CKSRYF105Z10
	C2042,C2045 (1.0F/5.5V)		PCH1132
	C4601 (10μF/50V)		VCH1224
	C4603 (3.3μF/50V)		VCH1225

RESISTORS

R1132,R1166,R1301,R1310,R1330	RS1/10S0R0J
R1350,R2188,R2189,R3241,R4410	RS1/10S0R0J
R1115	RS1/16S1501F
R3245,R3252	RS1/16S1801F
R1348,R3244,R3251	RS1/16S2201F
R1255,R1257,R1259	RS1/16S2701F
R1204,R1205,R1221,R1222	RS1/16S3300F
R1237,R1238	RS1/16S3300F
R1201,R1206,R1217,R1223,R1233	RS1/16S3301F
R1239	RS1/16S3301F
R1347	RS1/16S3901F
R1209,R1215,R1225,R1231,R1241	RS1/16S4700F
R1247,R3246,R3248,R3253,R3255	RS1/16S4700F
R1256,R1258,R1260,R3256,R3257	RS1/16S5601F
R4604	RS1/16S6202F
R1010,R1014,R1016,R1018	RS1/16S75R0F
R1020,R1021,R1041-R1043	RS1/16S75R0F
R1108	RS1/16S8200F
VR1311-VR1313,VR4101 (1kΩ)	ACP1089
Other Resistors	RS1/16S□□□J

OTHERS

X2002 (32kHz)	VSS1143
X2001 (6.25MHz)	VSS1162
CN2003 Connector 12P	12PL-FJ
CN3001 Connector	B10B-ZR
CN2001 Connector	B16B-PH-K
JA1401 Optical Link Out	GP1FA551TZ
CN2009 Connector 20P	HLEM20S-1
CN2006,CN2007 Plug 2P	KM200SA2
JA4501,JA4502 Jack	RKN1004
JA1411 Jack	VKB1074
CN2008 7P Connector	VKN1267
CN1001,CN1002 B to B Connector 24P	VKN1405
CN2010 20P Connector	VKN1424
CN1003 22P Connector	VKN1426
CN3002 Connector	VKN1626
1001 Screw Plate	VNE1948
KN3201-KN3204 Earth Metal Fitting	VNF1084
4101 TV Tuner Pack (USA)	VXF1005

B REAR JACK ASSY

SEMICONDUCTORS

Q1502	2SA1576A
Q1501,Q1503-Q1505	2SD2114K

RESISTORS

R1501,R1503,R1505,R1519,R1520	RS1/16S75R0F
R1524,R1531,R1532,R1535	RS1/16S75R0F
Other Resistors	RS1/16S□□□J

OTHERS

JA1501 3P Pin Jack	VKB1115
JA1521,JA1522 Jack	VKB1173

Mark	No.	Description	Part No.
	CN1501,CN1502	B to B Connector 24P	VKN1392
	1501	Screw Plate	VNE2247

**3D Y/C ASSY****SEMICONDUCTORS**

IC3101	MSM514265C-60TS
IC3201	TK15420M
IC3001	UPD64082GF-3BA
Q3002	2SA1576A
Q3001	2SC4081
Q3301	HN1B01FU
Q3305	HN1K03FU

COILS AND FILTERS

L3003	LCTA150J2520
F3001,F3002,F3101	VTF1170
L9001,L9002,L9023,L9301,L9302	VTL1081
L3001,L3106	VTL1096

CAPACITORS

C3337	CCSRCH100D50
C3350,C3351	CCSRCH101J50
C3022,C3023	CCSRCH151J50
C3027,C3029	CCSRCH180J50
C3013	CEAT100M50
C3017,C3025	CEAT101M10
C3006,C3101	CEAT471M6R3
C3305	CEJQ101M6R3
C3202	CEV101M16
C3004	CEV221M4
C3103	CKSRYB102K50
C3007-C3009,C3014-C3016	CKSRYB104K16
C3019,C3020	CKSRYB104K16
C3012,C3201,C3304,C3307	CKSRYF104Z25
C3001,C3003,C3005,C3010,C3011	CKSRYF105Z10
C3018,C3026,C3028,C3102	CKSRYF105Z10
C3104,C3105	CKSRYF105Z10

RESISTORS

R3016-R3019	RAB4C101J
R3307	RS1/10S0R0J
R3204,R3207	RS1/16S1501F
R3206	RS1/16S2201F
R3203	RS1/16S2701F
VR3301 (470Ω)	ACP1088
Other Resistors	RS1/16S□□□J

OTHERS

X3001 (20.000MHz)	ASS7023
CN3501 B to B Plug 30P	VKN1797
3001,3002 Screw Plate	VNE2247

**FRONT JACK ASSY****RESISTORS**

Other Resistors	RS1/16□□□J
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OTHERS

CN2002 Connector 12P	12R-FJ
CN2004 Connector	B6B-PH-K
JA2001 Y/C Connector	VKB1169
JA2002 Jack	VKB1170

Mark	No.	Description	Part No.
	JA2003	DV-Terminal	VKB1171
	KN2001,KN2002	Earth Metal Fitting	VNF1084

**MAIN ASSY****SEMICONDUCTORS**

△ IC2006	BA178M05FP
IC8005	BA4558F-HT
IC6004	CS8420-CS
IC5005	DVXCEL-BA1
IC1010	HD6417709AF100B
IC3008	HY57V641620HGT-7
IC1004	K4S643232E-TC60
IC7004	M32L1632512A-8Q
IC4003,IC4004	M5M4V18165DTP-6S
IC4007	M65774AFP
IC4001	MB81F161622C-80FN
IC4005	MB81F643242B-70
IC2002	MSM514800C-60JS
IC8006	NJM13404V
IC3007	NJM2115M
IC8011	PCM1716E
IC8003	PCM1800-1
IC8008	PD0272A
IC4006	PD6342A
IC9503	PDY078A
IC2004	PE5108A
IC3003	PE5219A
IC9501	PE7003C
IC6003	PE7004A
IC3001	PLL1700E
IC7006	PM0024AF
IC7003	PM0030A
△ IC1003,IC2008	PQ070XZ5MZP
△ IC2007	PQ12DZ51
△ IC7201	PQ2TZ15
IC3011	SN74AHC2G53HDCT
IC1011	TC554001AFT-70V
IC5003,IC5004	TC59S6432CFT-80
IC1007	TC74LCX16245AFT
IC1002,IC1005,IC1006,IC1009	TC74LCX541FT
IC1013,IC2001,IC3005	TC74LCX541FT
IC3010,IC9003	TC74LCX541FT
IC2005,IC6005,IC6006	TC74VHC14FT
IC3013	TC74VHCT08AFT
IC3014	TC74VHCT32AFT
IC2003	TC74VHCT541AFT
IC3002	TC74VHCU04FT
IC3012	TC7SH04F
IC3004,IC3006	TC7SLU04F
IC1001	TC7WU04FU
IC8002	TC9412AF
IC7005	TK15420M
IC9002	TSB41AB2PAP
IC9001	TSB42AB4PDT
IC8001,IC8010	UPC4570G2
IC6002	UPD61003
IC9502	UPD65954GC-E59-7EA
IC1008	VYW1898
Q7003-Q7009,Q8002,Q8006	2SA1576A
Q8001,Q8005,Q8008	DTC124EUA
Q1001	HN1K03FU

Mark	No.	Description	Part No.
	D8001-D8009		1SS355
	D5001		EC10QS04
	D5201,D5202		EP10QY03
	D3002		KV1832E

COILS AND FILTERS

F1101,F2101,F3101-F3103	DTF1069
F3110-F3112,F3117,F3124,F3127	DTF1069
F3132,F2062,F2065,F2102-F2105	DTF1070
F3128	DTF1070
F4101,F4103-F4106,F5106,F5107	DTF1070
L8004,L8005	LCYA100J2520
L3016	LCYA1R2J2520
F8007,F8008,F7014,F7015	VTF1150
F2006-F2009,F4006,F4010-F4012	VTF1171
F5002,F5009,F5011-F5013	VTF1171
F9002,F9003	VTF1171
L7014-L7016,L7020,L7021,L7023	VTL1075
L1004,L3013	VTL1078
L1002,L1005,L1006,L3004-L3009	VTL1079
L3014,L3015,L3018-L3022,L4002	VTL1079
L935,L936,L943,L944	VTL1082
L1003,L3031	VTL1084
L7017-L7019	VTL1086
L7003,L7004,L7006,L7008-L7010	VTL1124

CAPACITORS

C901-C908	CCSQCH4R0C50
C1201,C6041,C6046,C9026	CCSRCH102J50
C9001,C9002	CCSRCH120J50
C3036	CCSRCH220J50
C9025	CCSRCH221J50
C5051-C5068	CCSRCH470J50
C1014,C1015,C8016,C8017,C8124	CCSRCH471J50
C8129	CCSRCH471J50
C3037,C7107,C7112	CCSRCH5R0C50
C8123,C8131	CCSRCH750J50
C7091,C7093,C7095,C7105	CEV100M16
C2040,C2042,C7051,C8027,C8041	CEV101M16
C8121,C8126	CEV101M16
C2004,C2025,C2031,C2032,C2044	CEV101M6R3
C3016,C3025,C3026,C6043,C6044	CEV101M6R3
C8037,C8038,C8075,C8092,C8093	CEV101M6R3
C8096,C8097,C8109-C8111,C9012	CEV101M6R3
C9525	CEV101M6R3
C1003,C1004,C1007,C2023	CEV221M4
C2036-C2039,C3001-C3003	CEV221M4
C3013,C3040,C4001,C4002	CEV221M4
C4039-C4047,C4054,C5005	CEV221M4
C5007,C5008,C5022,C6004	CEV221M4
C6011,C6034,C7003-C7005	CEV221M4
C7025,C7034,C7039,C7065	CEV221M4
C7084,C7085,C8033	CEV221M4
C8001,C8004,C8005,C8007,C8008	CEV330M25
C8010,C8012-C8015,C8022	CEV330M25
C7010,C7027,C7028,C7042,C7043	CKSQYF225Z16
C7056	CKSQYF225Z16
C7078,C7100	CKSQYF475Z10
C4003,C5011,C5012,C5019,C5021	CKSRYB102K50
C5042,C8039,C8076	CKSRYB102K50
C2005,C2008,C2043,C3035,C5015	CKSRYB103K50
C5017,C5020,C5041,C5044,C6048	CKSRYB103K50
C6053,C7055,C8069	CKSRYB103K50

Mark	No.	Description	Part No.
	C8043,C8068,C8074		CKSRYB104K16
	C8067		CKSRYB105K6R3
	C6052		CKSRYB822K50
	C1001,C1002,C1008-C1013		CKSRYF104Z25
	C1016,C1017,C1019-C1044,C1046		CKSRYF104Z25

C1200,C2001-C2003,C2006	CKSRYF104Z25
C2009-C2011,C2014-C2022,C2024	CKSRYF104Z25
C2026-C2030,C2033-C2035,C2041	CKSRYF104Z25
C2045,C3004-C3012,C3014,C3015	CKSRYF104Z25
C3017-C3024,C3027-C3034,C3039	CKSRYF104Z25

C3041-C3050,C4004,C4008,C4010	CKSRYF104Z25
C4018-C4021,C4023,C4025	CKSRYF104Z25
C4030-C4034,C4048-C4053	CKSRYF104Z25
C4055-C4066,C4069-C4086	CKSRYF104Z25
C4088-C4118,C5001-C5004,C5006	CKSRYF104Z25

C5009,C5010,C5016,C5018	CKSRYF104Z25
C5023,C5024,C5027-C5040,C5043	CKSRYF104Z25
C5045-C5050,C5069-C5074,C6003	CKSRYF104Z25
C6005-C6010,C6012-C6033	CKSRYF104Z25
C6035,C6036,C6039,C6040,C6042	CKSRYF104Z25

C6045,C6047,C6055,C7023,C7076	CKSRYF104Z25
C7096,C7097,C7201,C7202,C8006	CKSRYF104Z25
C8026,C8029-C8032,C8036,C8040	CKSRYF104Z25
C8042,C8044,C8047-C8051	CKSRYF104Z25
C8057-C8061,C8070-C8072	CKSRYF104Z25

C8077,C8078,C8081-C8083	CKSRYF104Z25
C8085,C8086,C8089,C8091	CKSRYF104Z25
C8094,C8095,C8102,C8103	CKSRYF104Z25
C8107,C8108,C8112,C8122,C8127	CKSRYF104Z25
C9003-C9005,C9007,C9009-C9011	CKSRYF104Z25

C9013,C9015-C9017,C9019-C9024	CKSRYF104Z25
C9027,C9029-C9032,C9501-C9506	CKSRYF104Z25
C9508-C9519,C9521-C9524	CKSRYF104Z25
C9526-C9535	CKSRYF104Z25
C4005,C4006,C4015,C4016	CKSRYF105Z10

C4036,C4037,C7006-C7009,C7021	CKSRYF105Z10
C7024,C7035-C7038,C7041	CKSRYF105Z10
C7044,C7045,C7048-C7050,C7052	CKSRYF105Z10
C7054,C7059-C7064,C7067-C7074	CKSRYF105Z10
C7077,C7079-C7083,C7086-C7090	CKSRYF105Z10

C7092,C7094,C7099,C7102,C7103	CKSRYF105Z10
C7106,C7108-C7111,C7205,C8090	CKSRYF105Z10
C9014,C9018	CKSRYF105Z10
C6051	CKSRYF474Z16
VC3001 (20pF)	VCM1008

RESISTORS

R3067,R4054,R4071,R5015,R5016	RAB4C0R0J
R5023,R5024,R7081,R7089,R7115	RAB4C0R0J
R7119,R8082,R8095,R8103,R8121	RAB4C0R0J
R8136,R8137,R8146-R8148	RAB4C0R0J
R3137-R3142,R9017,R9018	RAB4C102J

R9026,R9027,R9567	RAB4C102J
R1025-R1028,R1031,R1032,R1046	RAB4C103J
R1050,R1067,R1071,R1079	RAB4C103J
R1095,R1096,R1115-R1122	RAB4C103J
R2033-R2035,R2040,R2060,R2064	RAB4C103J

R2074-R2078,R3001,R4086	RAB4C103J
R5105-R5109,R6029,R6034,R6039	RAB4C103J
R6043-R6045,R8047,R8048,R8118	RAB4C103J
R8133-R8135,R8143,R8144,R9009	RAB4C103J
R9056,R9065,R9066	RAB4C103J

R1033-R1036,R1039,R1041,R1044	RAB4C220J
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Mark	No.	Description	Part No.
	R1059,R1061,R1063,R1065		RAB4C220J
	R1069,R1070,R1072,R1077		RAB4C220J
	R1080-R1084,R1089,R1091		RAB4C220J
	R1097-R1106,R2023,R2024		RAB4C220J
	R2037,R2038,R2041,R2044,R2045		RAB4C220J
	R2050,R2056,R2058,R2059,R2061		RAB4C220J
	R2063,R2069-R2073,R3010		RAB4C220J
	R3019,R3025,R3032		RAB4C220J
	R3036,R3037,R3045,R3052		RAB4C220J
	R3061,R3062,R3064,R3073		RAB4C220J
	R3079,R3080,R3082,R3083,R3093		RAB4C220J
	R3114-R3118,R3120-R3123		RAB4C220J
	R3125-R3128,R4007,R4008		RAB4C220J
	R4010,R4011,R4015		RAB4C220J
	R4025,R4028,R4029		RAB4C220J
	R4041-R4043,4046-R4051,R4053		RAB4C220J
	R4056,R4059-R4062,R4066,R4068		RAB4C220J
	R4070,R4072,R4074-R4076,R4078		RAB4C220J
	R4080-R4082,R4084,R4085		RAB4C220J
	R4089,R4090,R4093-R4095		RAB4C220J
	R4097-R4104,R4106-R4111		RAB4C220J
	R5006-R5009,R5057,R5071,R5078		RAB4C220J
	R5084,R6002-R6007,R6021,R6022		RAB4C220J
	R6027,R6028,R6030,R6031,R6035		RAB4C220J
	R6037,R6040,R6041,R6046,R6047		RAB4C220J
	R6057,R6059,R6061-R6064,R6086		RAB4C220J
	R7042-R7044,R7056,R7061		RAB4C220J
	R7067,R7068,R9004-R9008,R9010		RAB4C220J
	R9019,R9021,R9029,R9031,R9032		RAB4C220J
	R9037,R9046,R9057,R9058,R9064		RAB4C220J
	R9067-R9072,R9509-R9512,R9517		RAB4C220J
	R9520-R9522,R9528,R9529		RAB4C220J
	R9536,R9537,R9540-R9542,R9545		RAB4C220J
	R9556,R9557,R9563-R9566		RAB4C220J
	R9569-R9571,R9573,R9574		RAB4C220J
	R9577-R9592		RAB4C220J
	R9033,R9034,R9041,R9042		RN1/16SC56R0D
	R1023,R2098		RN1/16SE1001D
	R8203,R8209		RN1/16SE1602D
	R2097		RN1/16SE3001D
	R8204,R8213		RN1/16SE3302D
	R1001,R1003,R1014,R1024,R1030		RS1/10S0R0J
	R1048,R1051,R1066,R1078,R1085		RS1/10S0R0J
	R1107,R2001,R2006,R2007		RS1/10S0R0J
	R2012-R2018,R2021,R2029-R2032		RS1/10S0R0J
	R2036,R2083-R2085,R2094		RS1/10S0R0J
	R3042,R3043,R3050,R3077,R3112		RS1/10S0R0J
	R45,R48,R49,R51		RS1/10S0R0J
	R53,R56,R6008,R6012,R6013		RS1/10S0R0J
	R6065,R6066,R6073,R6089,R7006		RS1/10S0R0J
	R7020,R7021,R7023,R7037,R7041		RS1/10S0R0J
	R7047,R705,R7065,R707		RS1/10S0R0J
	R7085,R7086,R7111,R713,R7201		RS1/10S0R0J
	R724,R8001,R8012,R8015		RS1/10S0R0J
	R8024,R8025,R8039,R8040,R8063		RS1/10S0R0J
	R8168,R8205,R9011,R9073,R9507		RS1/10S0R0J
	R9527,R9568		RS1/10S0R0J
	R5067		RS1/10S100J
	R2022,R2026,R2027		RS1/10S101J
	R5066		RS1/10S150J
	R7099		RS1/10S220J
	R7022,R7075,R8094		RS1/16S1001F

Mark	No.	Description	Part No.
	R8090		RS1/16S1002F
	R8037		RS1/16S1003F
	R8091		RS1/16S1301F
	R7104,R7133		RS1/16S1501F
	R8080		RS1/16S1802F
	R8073,R8107		RS1/16S2201F
	R7103,R7132		RS1/16S2701F
	R7102,R7110,R7131		RS1/16S3300F
	R8093		RS1/16S3601F
	R1012,R7026,R7076		RS1/16S3900F
	R8074,R8116		RS1/16S5600F
	R9022		RS1/16S6341D
	VR7003-VR7005 (100Ω)		VCP1167
	VR7006,VR7007 (470Ω)		VCP1169
	Other Resistors		RS1/16S□□□J

OTHERS

X1001 (40MHz)		DSS1101
X3002 (54.000MHz)		VSS1138
X3001 (27.000MHz)		VSS1146
X9001 (24.576MHz)		VSS1151
X5001 (27.500MHz)		VSS1153
CN8001	Connector	B10B-ZR-SM3
CN2003	Connector	B14B-PH-SM3
CN2002	Connector	B4B-ZR-SM3
CN9001	Connector	B6B-PH-SM3
CN6001	Connector	B6B-ZR-SM3
CN1002	7P Connector	NS-U005
CN2001	20P Connector	VDA1681
CN7001	22P Connector	VKN1411
		VKN1424
		VKN1426
CN3001	40P FFC	VKN1786
KN1-KN6	Earth Metal Fitting	VNF1109

FL ASSY

SEMICONDUCTORS

IC1201		MSM9202-01
Q1601		2SB1238X
Q1201,Q1501-Q1505		DTC124EUA
D1601,D1602		1SS355
D1505		LNG989CNBW
D1501,D1503,D1603		UDZ12B
D1506		UDZS6.2B

COILS AND FILTERS

L1601		LRCA100J
L1201		LRCA220J

SWITCHES AND RELAYS

S1301-S1307		ASG7013
-------------	--	---------

CAPACITORS

C1206-C1208		CCSRCH101J50
C1209		CCSRCH390J50
C1210,C1603		CEAT100M50
C1203,C1212		CEAT101M10
C1605		CEAT101M16
C1402		CEJQ221M10
C1301,C1403,C1501,C1606		CKSRYB103K50
C1211,C1601,C1602		CKSRYF103Z50
C1205,C1213		CKSRYF104Z25
C1204		CKSRYF105Z10

DVR-7000

Mark	No.	Description	Part No.
RESISTORS			
	Other Resistors		RS1/16S□□□J
OTHERS			
	CN1203	Connector 4P	04R-FJ
	CN1204	Connector 7P	07R-FJ
	CN1201	Connector Post	B7B-PH-K
	1401	Remote Receiver Unit	GP1U28X
	CN1202	Connector 20P	HLEM20S-1
	V1201	Fluorescent Tube FL Spacer FL Holder	VAW1067 VEB1125 VNF1087

G JOG ASSY

SEMICONDUCTORS

Q1101	DTC124EUA
D1101	SLR-343VC

SWITCHES AND RELAYS

S1102	ASG7013
S1101	VSX1002

CAPACITORS

C1101,C1102	CKSRYB103K50
-------------	--------------

RESISTORS

Other Resistors	RS1/16S□□□J
-----------------	-------------

OTHERS

CN1101	Connector 7P	07P-FJ
--------	--------------	--------

H SW ASSY

SWITCHES AND RELAYS

S1001	ASG7013
-------	---------

CAPACITORS

C1001	CKSRYB103K50
-------	--------------

RESISTORS

Other Resistors	RS1/16S□□□J
-----------------	-------------

OTHERS

CN1001	Connector 4P	04PL-FJ
--------	--------------	---------

I POWER SUPPLY ASSY

SEMICONDUCTORS

△ IC271,IC301	VZF1089
△ IC801,IC910	VZF1107
Q252,Q272,Q410,Q911	2SC1740
Q312	2SC2655
Q313	DTC114ES
Q314	DTC143ES
Q120	VZF1101
Q110	VZF1108
Q211	VZF1109
Q221	VZF1110
Q251	VZF1111

Mark	No.	Description	Part No.
	Q271,Q910		VZF1112
	Q412		VZF1113
	Q111,Q122,Q131,Q501		VZF1114
	Q311		VZF1115
	D134,D220,D311,D424		10ELS2
	D112,D122,D252,D453		1SS270A
	D211		MTZJ39D
	D103		UK1V26
	D212		VZF1045
	D611		VZF1051
	D210,D410		VZF1053
	D612		VZF1057
	D101		VZF1063
	D901		VZF1075
	D701		VZF1081
	D451,D452		VZF1083
	D251,D801		VZF1087
	D510,D511		VZF1088
	D127		VZF1100
	D110,D123		VZF1105
	D222,D224		VZF1118
	D421-D423		VZF1119
	TH451 Thyristor(3P4J)		VZF1117
	PC101-PC103,PC501 Photo Coupler		VZF1116

RESISTORS

△ R410	Fusible Resistor(10Ω)	VZC1063
R212	Fusible Resistor(47Ω)	VZC1065

OTHERS

△ P221,P226	Fuse(1A)	VEK1041
△ P610	Fuse (0.75A)	VEK1042
△ P252,P611	Fuse (1.5A)	VEK1048
△ P271,P701,P915	Fuse (2.5A)	VEK1056
△ P815	Fuse (3.5A)	VEK1073
△ FU101	Fuse (3.15A)	VEK1044

■ (REFERENCE) RECORDER DRIVE MAIN ASSY CONTRAST TABLE

This service manual does not include ASSY PARTS LIST of the RW RECORDER SECTION.
But as a reference, the CONTRAST TABLE between the RECORDER DRIVE MAIN ASSY of DVR-7000 and DVR-A03 are listed as following.

DWX2148 and DWX2147 are constructed the same except for the following:

Mark	Symbol and Description	Part No.		Remarks
		(DVR-A03) DWX2147	(DVR-7000) DWX2148	
	IC100 IC111 IC110 IC113 IC303,305	Not used UPD72153GM-UEU EL6257CU PCM1719E TC4W53FU	TC7WH08FU UPD72153AGM-UEU Not used Not used Not used	*
	IC306 IC501 IC502 IC503 Q102,Q103	M37902FGCHP SM8706AV K4E151612D-TL50 RL5E839 HN1B04FU	M37911FGCHP SM8706BV Not used Not used Not used	
	Q106 Q107-Q110,Q401 D101-D104 L105-L108 L1000,L1001	DTA114EK 2SD2114K 1SS355 PTL1014 DTL1087	Not used Not used Not used Not used Not used	
	L1011,L1012,L1100,L1108-L1110 C95 C100 C131 C154,C163,C175	Not used Not used Not used CKSRYB102K50 CKSRYF104Z25	VTL1079 CKSRYB105K6R3 CKSRYF104Z25 CCSRCH221J50 CKSRYB105K6R3	* * *
	C138,C146 C169,C172 C93,C94 C102,C105 C104,C197,C306,C307,C502-C507,C515	CKSRYF105Z10 CCSRCH221J50 CKSRYB102K50 CKSRYB104K16 CKSRYF104Z25	CKSRYB105K6R3 Not used Not used Not used Not used	
	C516,C519,C522,C524-C532,C1102 C1108,C1112,C1113,C1123,C1124 C170 C193 C179-C183	CKSRYF104Z25 CKSRYF104Z25 CKSQYF225Z16 CKSRYB103K50 CKSRYB104K16	Not used Not used Not used CKSRYB104K16 CCSRCH471J50	
	C518 C521 C517 C520 C501	CKSRYB472K50 CKSRYB562K50 CKSRYB393K16 CKSRYB473K16 CKSQYF225Z16	Not used Not used Not used Not used Not used	
	C523 C807 C1103,C1109 C1114,C1115,C1122 C1137,C1138(4.7mF/16V)	CKSQYF225Z16 CKSRYF104Z25 CEV100M16 CEV470M6R3 DCH1142	Not used CKSRYB104K16 Not used Not used Not used	
	C1110,C1111 C1131 C1116,C1117 C1024,C1025 R98,R99	CKSRYB122K50 CKSRYF103Z50 CKSRYF224Z16 Not used Not used	Not used Not used Not used CKSRYB102K50 RS1/10S0R0J	* *
	R100,R341,R342,R414,R1120,R1122 R1123,R1124,R1126,R1128 R109 R156 R109	Not used Not used RS1/16S151J RS1/16S680J RS1/16S151J	RS1/16S0R0J RS1/16S0R0J RS1/16S221J RS1/16S220J RS1/16S221J	* *

Mark	Symbol and Description	Part No.		Remarks
		(DVR-A03) DWX2147	(DVR-7000) DWX2148	
	R188 R150 R194 R104,R105,R119,R189,R195,R196 R158,R164,R174,R177,R182,R197,R1102	RS1/16S222J RAB4C103J RS1/16S180J RS1/16S102J RS1/16S222J	RS1/16S0R0J Not used Not used Not used Not used	
	R187 R185,R193,R520 R106,R110 R180,R186 R232,R519,R530,R1121,R1125,R1127	RS1/16S392J RS1/16S103J RS1/16S473J RS1/16S104J RS1/16S0R0J	Not used Not used Not used Not used Not used	
	R531 R509,R510 R523,R524 R518 R521,R522,R532,R1100,R1107-R1110	Not used RS1/16S220J RS1/16S470J RS1/16S510J RS1/16S101J	RS1/16S103J Not used Not used Not used Not used	*
	R516 R514 R517 R515 R511,R512	RS1/16S431J RS1/16S821J RS1/16S302J RS1/16S432J RAB4C330J	Not used Not used Not used Not used Not used	
	R923 R1013 R1014 R1101 R1114	RS1/16S391J Not used Not used RS1/16S180J RS1/16S511J	RS1/16S471J RS1/16S471J RS1/16S101J Not used Not used	* *
	R1112 R1113 R1105 R1129-R1132 VR105 (10KΩ)	RS1/16S151J RS1/16S333J RS1/16S105J RS1/16S0R0J DCP1080	RS1/16S471J RS1/16S0R0J Not used RS1/16S221J Not used	
	CN403 (Connector) CN405 (Connector 6P) CN406 (Connector)) CN407 (Connector 6P) CN409 (40P Flexible Connector)	Not used Not used Not used Not used Not used	S6B-PH-SM3 DKN1224 S4B-ZR-SM3A S6B-ZR-SM3A DKN1230	* * * * *
	JA101(Jack) CN401 (LK Connector) CN402 (ZH Connector 2P) CN408 (2P Digital Out Connector)	DKN1123 LK-44104H-S1D1Z-2 B2B-ZR-SM3 DKN1176	Not used Not used Not used Not used	

* : Additional parts for DWX2148

6. ADJUSTMENT

6.1 3D Y/C ASSY ADJUSTMENT

No.	Adjustment Name	Adj. Point	Measurement Point	Adjustment Value	Adjustment State
1	Y/C input level adjustment (Input system adjustment)	VR3301	TUMJ ASSY CN3001 Pin10(SEL Y)	2.00Vp-p $\pm$ 80mV	Input a white 100%(1.0Vp-p) signal into Input 1 (composite). (75 Ω termination)

6.2 TUMJ ASSY ADJUSTMENT

6.2.1 TUMJ ASSY ADJUSTMENT TABLE

Note : Use disc : [DVD test disc GGV1025]

No.	Adjustment Name	Adj. Point	Measurement Point	Adjustment Value	Adjustment State
1	Video level adjustment of terrestrial wave (Input system adjustment)	VR4101	TUMJ ASSY CN3001 Pin10(SEL Y)	2.00Vp-p $\pm$ 80mV	Input a signal of fv=EIA color-bar 60dB μ V to terrestrial wave input. /through output.
2	Audio multiplex ATT adjustment (Input system adjustment) Refer to 6.2.2.	IC4601 (IIC bus adj.)	Audio ouput (R) (Rear panel)	310mVrms $\pm$ 9.3mV	Input a signal of Mono 1kHz/100% modulation to terrestrial wave input. /through output. (Rec level = $\pm$ 0) Note 2
3	Audio multiplex WIDE BAND adjustment (Input system adjustment) Refer to 6.2.2.	IC4601 (IIC bus adj.)	Audio ouput (R) (Rear panel)	Best point of separation $\geq$ 30dB Note 1	Input a signal of Stereo 300Hz/30% modulation (NR-ON) to terrestrial wave input. /through output Note 2
4	Audio multiplex SPECTRAL adjustment (Input system adjustment) Refer to 6.2.2.	IC4601 (IIC bus adj.)	Audio ouput (R) (Rear panel)	Best point of separation $\geq$ 25dB Note 1	Input a signal of Stereo 3kHz/30% modulation (NR-ON) to terrestrial wave input. /through output Note 2
5	Y level adjustment of component system (Output system adjustment)	VR1311	Component ouput (Y) (75 Ω terminate)	1.0Vp-p $\pm$ 40mV	100% white data playback (DVD-REF-A1 T2-C5,etc)
6	Pb level adjustment of component system (Output system adjustment)	VR1313	Component ouput (PB) (75 Ω terminate)	714mVp-p $\pm$ 28mV	100% white data playback (DVD-REF-A1 T2-C19,etc)
7	Pr level adjustment of component system (Output system adjustment)	VR1312	Component ouput (PR) (75 Ω terminate)	714mVp-p $\pm$ 28mV	100% white data playback (DVD-REF-A1 T2-C19,etc)

Note 1 : The values for channel separation is defined as those having passed through the following filters :

100Hz – 10kHz : +0/–0.5dB

15.75kHz – 100kHz : -40dB or more

Note 2 : The audio multiplex adjustment No.2 – No.4 is done under the debugging mode.

Refer to 6.2.2 about the details.

6.2.2 AUDIO DEMULTIPLEX ADJUSTMENT MODE

This section describes how to set the each parameter of US Audio Multiplex Decoder IC (CXA2094Q) on the TUMJ ASSY and memorize the data on the EEPROM in the TUMJ ASSY.

The adjustable parameters and setting data are following :

- ATT 00 ~ 15
- Wideband 00 ~ 63
- Spectral 00 ~ 63

■ How to Setting

■ Use Service Remote Control Unit [GGF1067]

● How to Enter the Audio Demultiplex Adjustment Mode

Press the [ESC] and [P.RUN] buttons sequentially.
Then the screen turns to Audio Demultiplex Adjustment Mode, and displays the following screen.

①
②
③

< Tuner Audio Separation Adjustment >

ATT >>>>>>>> 09

Wideband >>>>> 31

Spectral >>>>> 31

*** How to operate ([Button : Action]) ***
[SPEED-, SPEED+ : Adjust ATT]
[SCAN<<, SCAN>> : Adjust Wideband]
[STILL STEP<|, STILL STEP|> : Adjust Spectral]
[PLAY : Memorize the present status on TUFL-EEPROM]
[ESC : Exit]

● How to Change the Parameter

- ① ATT Increase or decrease the setting data by [SPEED+] or [SPEED-]
- ② Wideband Increase or decrease the setting data by [SCAN>>] or [SCAN<<]
- ③ Spectral Increase or decrease the setting data by [STILL STEP|>] or [STILL STEP<|]

The level display(bar-graph) and setting data are displayed at the right side of each item.

● How to Memorize the Setting Data

Press the [PLAY] key of GGF1067 to memorize the data on the EEPROM in the TUMJ ASSY after setting each parameter.
(The data is not erased even if the AC plug is disconnected from the outlet.)

● How to Exit the Audio Demultiplex Adjustment Mode

Press the [ESC] key of GGF1067 to exit the Audio Demultiplex Adjustment Mode.
Then the mode screen disappears.

6.3 MAIN ASSY ADJUSTMENT

Note : Use disc : [DVD test disc GGV1025]

No.	Adjustment Name	Adj. Point	Measurement Point	Adjustment Value	Adjustment State
1	Master clock free-running adjustment (Clock system adjustment)	VC3001	MAIN ASSY IC4007 Pin54 (CLKO) (M65774AFP)	27.000000MHZ ± 130Hz	No input signal or during test disc play-back
2	Y level adjustment of CVBS system (Output system adjustment)	VR7006	Y output of S terminal (75Ω termination)	1.00Vp-p ± 40mV	Playback the DVD test disc(100%white). Terminate the Y output of S terminal with 75Ω and adjust so that the level of between sync tip and white peak becomes 1.0Vp-p.
3	C level adjustment of CVBS system (Output system adjustment)	VR7007	C output of S terminal (75Ω termination)	286mVp-p ± 11mV	Playback the DVD test disc(100%color- bar). Terminate the C output of S terminal with 75Ω and adjust so that the amplitude of color burst becomes 286mVp-p.
4	Y level adjustment of component system (Output system adjustment)	VR7003	MAIN ASSY CN7001 Pin11 (Y Out)	800mVp-p ± 24mV	Playback the DVD test disc(100%white). At the pin 11 of CN7001 in the MAIN ASSY, adjust so that the level of between sync tip and white peak becomes 0.8Vp-p.
5	Pb level adjustment of component system (Output system adjustment)	VR7004	MAIN ASSY CN7001 Pin13 (Pb Out)	760mVp-p ± 22mV	Playback the DVD test disc(100%color- bar). At the pin 13 of CN7001 in the MAIN ASSY, adjust so that the level of between bottom and top becomes 0.76Vp-p in the 100% color-bar screen.
6	PR level adjustment of component system (Output system adjustment)	VR7005	MAIN ASSY CN7001 Pin15 (PR Out)	760mVp-p ± 22mV	Playback the DVD test disc(100%color- bar). At the pin 15 of CN7001 in the MAIN ASSY, adjust so that the level of between bottom and top becomes 0.76Vp-p in the 100% color-bar screen.

E MAIN ASSY

SIDE A

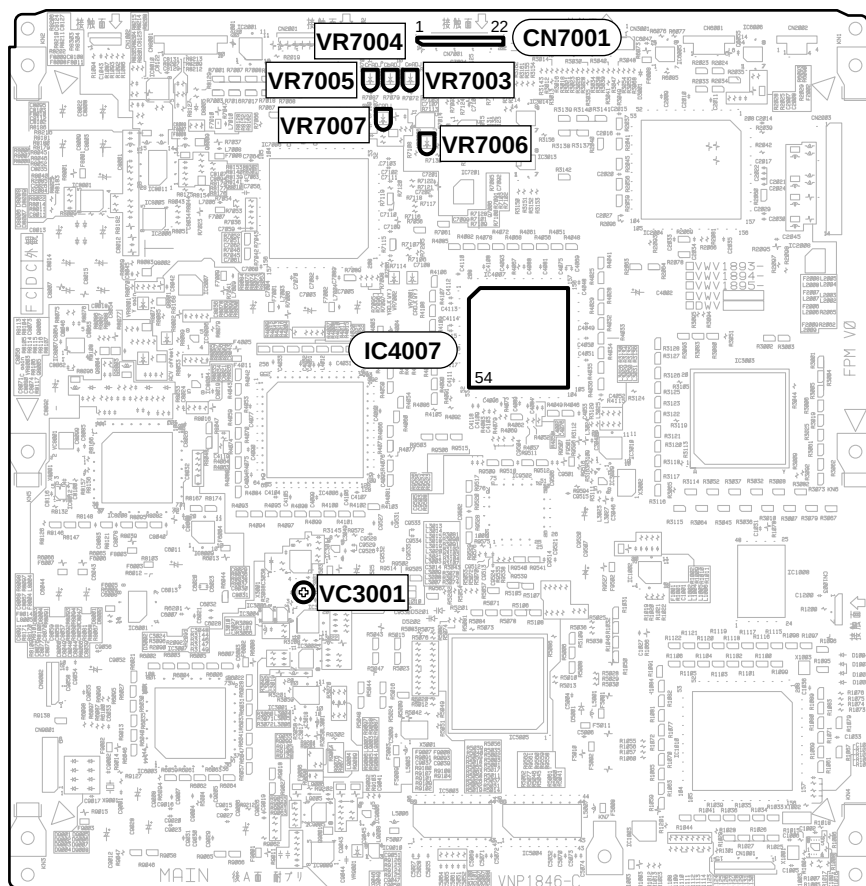


Fig.2 Adjustment Point

7. GENERAL INFORMATION

7.1 DIAGNOSIS

7.1.1 MODEL TYPE AND REGION SETTING

■ Setting the Model type and Region No. for DVD Recorder

For the DVD recorder DVR-7000/KU/CA and /LB type, it is necessary to set the region No. [1 or 3] on the FLASH ROM in the MAIN ASSY and the model type [KU or LB] on the EEPROM in the TUMJ ASSY. So when the MAIN ASSY or TUMJ ASSY is renewed, "The Model type and Region setting mode screen" is displayed automatically.

Note : If the region No. is once set, it is unable to rewrite it. When it is necessary to change the region No., renew the MAIN ASSY. And it is able to rewrite the once set model type on the EEPROM in the TUMJ ASSY only when the MAIN ASSY is renewed and setting the new region No. on the FLASH ROM.

● How to set the Model type and Region No.

1. Turn the power on.
2. The setting request screen is displayed when the model type and region No. is not set.
At this time FL displays " MODE SETTING".

[Recorder's Model and Region Setting] Please pick out any one of the following.		
Button No.	Model	Region
[1	: KU_MODEL<North America>	Region 1]
[2	: LB_MODEL <Taiwan>	Region 3]

3. Enter the data according to the mode menu by the service remote control unit.
4. The recorder restarts automatically.
5. Set the shipping position. (stop + power off)
But it is omitted when making the Down Load of the system μ -com is done after this.
6. Turn off the power, then turn on the power again.

● When the FL displays "MODEL MISMATCH" after connecting the AC plug to the outlet.

It displays, connecting the AC plug to the outlet when the setting is mismatched between the software setting of the model type data on the EEPROM and the μ -com hardware pin setting of the model type in the TUMJ ASSY.

At this time, it is unable to turn on the power.



It is considered the TUMJ PCB board fault (model type hardware pin setting fault).

Note : [Tuner control μ -com hardware pin setting of the model type]

Pin 76=Region 1, Pin 77=Region 2, Pin 98=Region 3

Pull up the correspond pin to Vcc(V+3_3M) and pull down other setting pins to GND by 10k Ω resistor.

● When the screen shows the following display after turning on the power

<display 1>

< Model and Region don't match >
 Model [already memorized on the TUFL-EEPROM] : KU_MODEL
 Region [already memorized on the MAIN-CPU-FLASH ROM] : 3
 Please take the power-plug off
 the plug socket

model type information in the TUMJ ASSY

region information memorized in the MAIN ASSY

It displays, exchanging the MAIN ASSY or TUMJ ASSY, etc when the combination of model type and region No. already set is mismatched.

After this, it is unable to operate any functions.



Match the combination between the model type and region No. setting, or renew the ASSY and set the data newly.

● When the screen shows the following display after setting the Model type and Region No.

<display 2>

< You can't change and overwrite the Region No. ! >
 Region was already memorized on the MAIN-CPU-FLASHROM
 and you can't overwrite the different Region.
 Region[already memorized on the MAIN-CPU-FLASHROM] : 3
 Model-Region[that you selected just now] : KU_MODEL -1
 Please take the power-plug off
 the plug socket.

region information memorized in the MAIN ASSY

region information selected by the key input at the setting mode screen

It displays, renewing TUMJ ASSY, etc when setting the different model type from the region No. already set in the FLASH ROM in the MAIN ASSY.



Match the combination between the model type and region No. setting, or renew the MAIN ASSY and set the data newly.

7.1.2 CPRM ID NUMBER AND ID DATA SETTING

■ Use ID DATA DISC [GGV1065] and Service Remote Control Unit [GGF1067]

■ Entering the ID Number and ID Data for DVD Recorder

For the DVD recorder, it is necessary with the recoding/playback of DVD-RW disc to set an individual number (ID number) and ID data to each recorder. If the number and data are not set correctly with the following procedure, operations in the future may not be guaranteed. You will find the ID number to be set on the ID label on the rear panel.

Important: If no ID label is found on the rear panel, write down the specified ID number by checking it according to "How to confirm the ID number" shown below.

■ The Input is Necessary When:

- "CPRM ERR" is displayed on the FL display immediately after the power is turned on or in Stop mode.
- When the MAIN ASSY, RECORDER DRIVE MAIN, CPRM LSI or the FLASH ROM is exchanged.

Note:

Be sure to enter the ID number in Stop mode.

Use the service remote control (GGF1067) for operations. Only opening/closing of the tray are performed from the player.

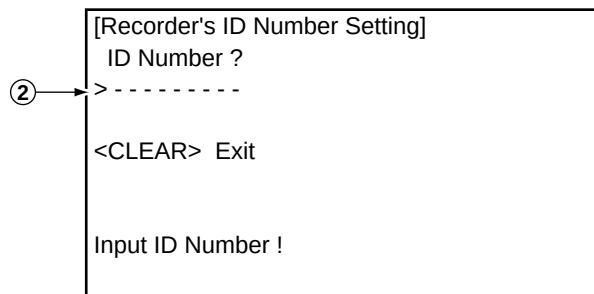
The ID data disc is swept out automatically after the recorder have read the data from it.

■ How to Input the ID Number and ID Data

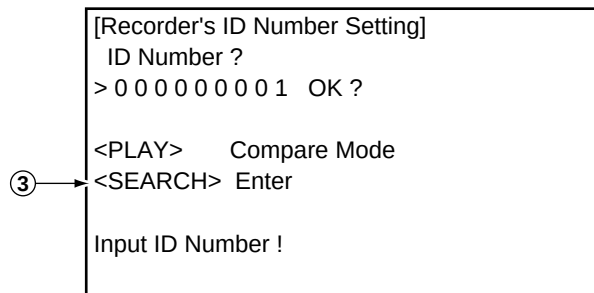
- ① To enter the input mode, press **[ESC]** + **[STEREO]** in a status with no ID number set, such as after FLASH-ROM downloading.



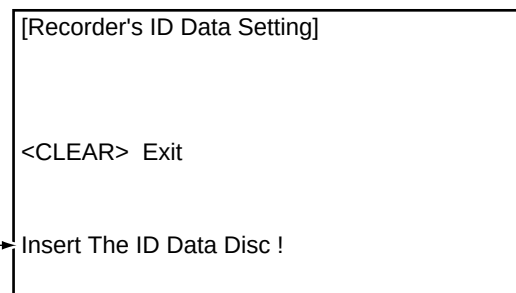
- ② As number input is enabled when the unit enters the input mode, input the 9-digit ID number.
(The entered number is also displayed on the FL display.)



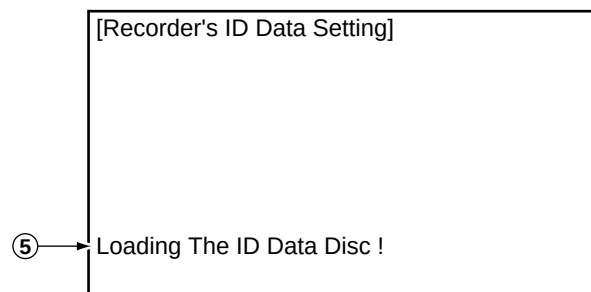
- ③ After inputting the number, press **[SEARCH]** to register the ID number.



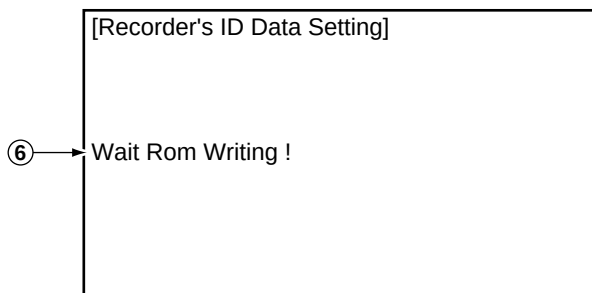
- ④ When the ID number has been registered, the unit enters the ID data input mode. (The FL display indicates "INSERT ID DATA.") In this condition, place the ID data disc on the tray and close the tray using the CLOSE key "■/▲" on the player.



- ⑤ While the data are being read, the message shown in the figure at left is displayed on the screen. (The FL display indicates "LOAD ID DATA.")

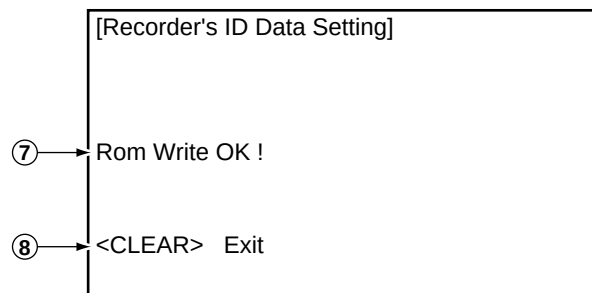


- ⑥ When the ID data have been read, the data are written to the FLASH-ROM.
(The FL display indicates "WRITE ID DATA.")



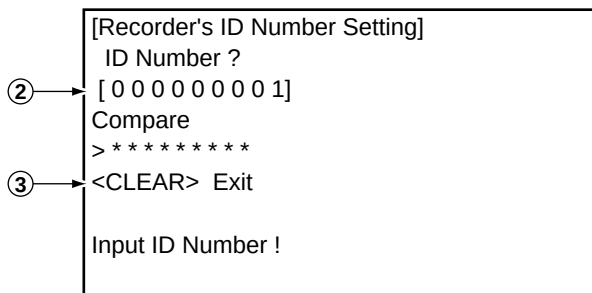
- ⑦ When the ID data have been written to the FLASH-ROM, the message "Rom Write OK" is displayed on the screen.
(The FL display indicates "ID DATA OK.")

- ⑧ After confirming this message, press **CLEAR** to exit the input mode.



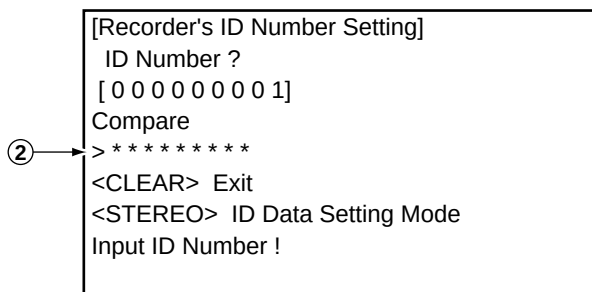
How to Confirm the ID Number

- ① Press **ESC** + **STEREO** with an ID number set, and the unit enters the ID number confirmation mode.
② The set ID number is displayed on the screen (and on the FL display), permitting you to confirm it.
③ To exit this mode, press **CLEAR**.

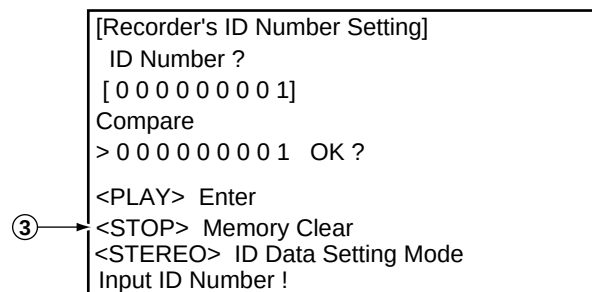


How to Clear the ID Number

- ① Press **ESC** + **STEREO** with an ID number set, and the unit enters the ID number confirmation mode.
② Input the same number as the ID number you have set.



- ③ After inputting the number, press **STOP**.
Only when the entered number matches the set ID number, the ID number is cleared and the unit exits this mode.
If the numbers do not match, you must return to step 2.
(**STOP** is not accepted until 9 digits are entered.)



7.1.3 DEBUGGING MENU

For operation, use the **GGF1067** remote control unit for service.
The Debug menu is a main menu from which to select any of 11 mode menus, classified by rough category, such as recording system and VR playback system. The mode menus also have subscreens if there are many items.
The Debug menu during playback of a DVD-V (including video mode), CD, or VCD is almost the same as that of the DV-737 (see Mode Menu 10).

- **How to Enter the Debug Menu** : Press **[ESC] + [DISP]** keys in order while no GUI is displayed.
- **How to Exit the Debug Menu** : Press the **[ESC]** key.
- **How to Advance the Mode Menu** : Press the **[DISP]** key.
- **How to Advance the Subscreen in a Mode Menu** : Press the **[DIG/ANA]** key.

Note 1 : If you press the [DISP] key on the final mode menu, the display will return to Mode Menu 1.
Note 2 : Pressing the [DIG/ANA] key repeatedly will change the subscreens within the same mode cyclically. To change mode menus, press the [DISP] key.

■ Description of Each Mode
1. Mode Menu 1 [Version information, etc.]

● Subscreen 1

① DVR-7000 /KU

② SYSCON : RELEASE_1 1 2

③ Rev : 1. 6 1 0 9. 2. 2 2 6. 2. 4

④ TUFLCON : 1. 5 2 0 0

⑤ DRIVE : PIONEER

DVD-RW DVR-7 0 0 0

1. 6 1 C 7 9 1 1

A E T 0 0 0 0 2 2 4 J P

⑥ DEVICE : AV1=ES6. 0

⑦ REGION : 1

\$

OK

OK

OK

OK: Correct combination

NG+: Version of the tuner microcomputer too high

NG-: Version of the tuner microcomputer is too old

OK: Correct combination

NG+: Version of the drive too high

NG-: Version of the drive is too old

OK: Serial No. of the drive is Registered

NG: Serial No. of the drive is not Registered

- ① Model name/destination
- ② Version of the recorder software
- ③ Revision No. of the system control computer software
- ④ Version No. of the tuner microcomputer, result of confirmation on combination between the tuner microcomputer and the system control computer
- ⑤ Information on the built-in drive (Name of the manufacturer, model name of unit into which the drive is built, version No., CPU model name, serial No., result of confirmation of combination with the system control computer*2)
- ⑥ Version No. of AV1
- ⑦ Region No.

● Subscreen 2

① ERR RATE : x. x x E-x /

- ① Error rate during playback in VR mode (Averaging value for last 10VOBUs),
Display the rotation ratio of the drive (/: Normal speed, No display: Double speed)
Note: Be sure to start playback after displaying this screen.

2. Mode Menu 2 [VR playback (related to decoding), debug display]

● **Subscreen 1** (This menu is for design use.)

● Subscreen 2

Error history of VR playback

① G:01-01 00m00s00#-. -e-- 00000000
 m_s_Message m_s_Er
 G01:0000 Tr:SchLate G01:0000 80
 L02:1230 Tp:VobDif+ L02:4103 -C0
 L02:4104 Tp:VobDof-
 ② ③

- ① Information on location of the display

Original (G)/Play List (L), title, chapter [X:XX-XX], time of the display (min, sec, frame) [XXmXXsXX], busy mark of the virtual mechanical control computer [#], error rate of the transfer data [X.XeXX], playback logical address (ID) [XXXXXXXXXX]

- ## ② Error Message history

Original (G)/Play List (L), title, time of occurrence (min, sec) [XXX:XXXX], playback-related error history for the last 8 errors [XX:XXXXXXXX]

Note:

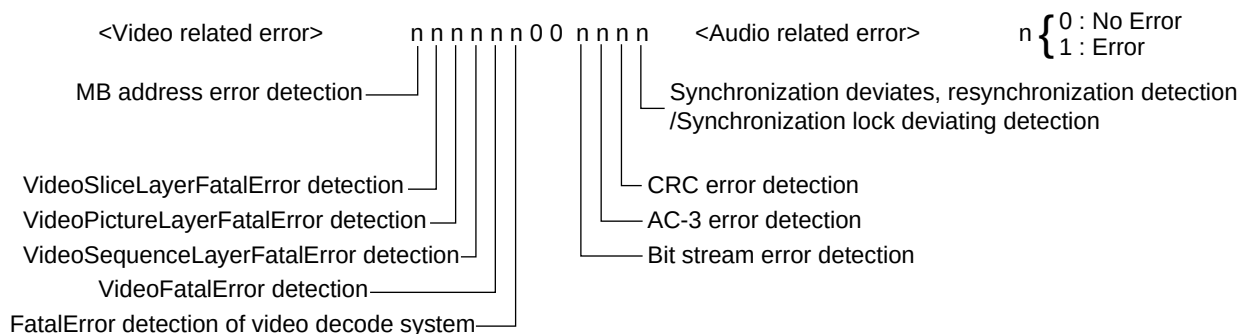
- For details on error information, see Table 7.1 “Description of VR playback-related errors,” page 92.

- When an error occurs here, expect that there is a problem in data reading from the disc.

(The possibility that there is a problem in the drive side is high.)

- ### ③ AV1 error status history

Original (G)/Play List (L), title, time of occurrence (min, sec) [XXX:XXXX], AV1 error status [XXX]. (The details are as follows.)



Note:

- When there is not an error of ②, and an error of ③ occurs here, there is a problem in the AV side.

(The possibility that there is a problem in AV1 tip or DVxcel is high.)

- When there is not an error of ② and ③ together, the screen is frozen and a sound breaks off, the possibility that a source itself is such a thing is high, and it is most of not to be trouble.

● **Subscreen 3** (This menu is for design use.)

3. Mode Menu 3 [iLink-related debug display]

● Subscreen 1

①	[Recorder]	GUID : XXXXXXXXXXXXXXXX
②	BGC : XXXX	TN : XX DN : XX CA : X ER : X
③	CT : XXXX	CD : XX CG : XX OC : X IC : X
④	PE : XXXX	
①	[DV]	GUID : XXXXXXXXXXXXXXXX
⑤	VN : XXXXXXXXXXXXXXXX	MN : XXXXXXXXXXXXXXXX
⑥	PW : XX TRM : XX TRS : XX	

- ① GUID Show the Global Unique ID (EUI-64)
- ② BGC Show the bass reset processing number of times
TN Show the existing i.LINK equipment total number on the same bass. (Include recorder)
DN Show the existing DV equipment total number on the same bass
CA Show whether there are data in the stream buffer of 1394 LINK chip [Y/N]
ER Show whether an error occurred in the driver section.
- ③ CT Show format of the connection that recorder organized [BROAD/PTOP]
CD Show format of the connection that recorder organized [IN/OUT]
CG Show whether a broadcast-out connection was taken by other equipment
OC Show number of a connection organized to Output Plug
IC Show number of a connection organized to Input Plug
- ④ PE Show number of the packet error that detected by 1394 LINK chip
- ⑤ VN Show Vendor Name of DV equipment
MN Show Model Name of DV equipment (There is the case that cannot get by equipment.)
- ⑥ PW, TRM, TRS
 Show the various state that got from DV equipment (Do not get it except DV input selection time.)

4. Mode Menu 4 [DVxcel-related debug display]

● Subscreen 1, Subscreen 2

(These menus are for design use.)

5. Mode Menu 5 [Mode-related debug display]

● Subscreen 1– 7

(These menus are for design use.)

6. Mode Menu 6 [VR recording-related debug display]

● Subscreen 1– 3 (These menus are for design use.)

● Subscreen 4

Error history of VR recording

①	Recording Error History Display
	01-06-01 20:05:30 No SysHdr IN
	01-06-02 00:22:10 Write Error

- ① Recording-related error history of the last 9 times × 2 pictures
[occurrence time (yr-mo-day hr:min:sec), error information (in simplified description)]

Notes:

- The two error-history pages can be switched by pressing the [SPEED +] or [SPEED –] keys.
- For details on error information, see Table 7.2 “Description of VR recording-related errors,” page 93.

● Subscreen 5– 11 (These menus are for design use.)

7. Mode Menu 7 [VR playback-related debug information]

● Subscreen 1– 3

①	G01-01	Ep01	00:20'13"00
	Vrplay	000 Flgw	Rev : 1, 55, 8, 3
	Err		
	Read	Flgw	Flg : 0000a
	DIRd - Slep	DMA-Dnnl	Flg : 00801
	Spd : 01-000	8.25E-5/	Enp :8
②	Lsn:057a00	Err : 6.93E-5	Tn:0053n
	057a80	8.41E-5	0054
	057b80	6.27E-5/	0053
	057ba0	6.60E-5	0054

- ① Display position information
Original (G)/Play List (L), title No., cell No. [XXX-XX], chapter (entry point) [EpXX], time of the display (min, sec, frame) [XX:XX'XX"XX]
- ② Error rate information (four histories)
Logical address [Lsn:XXXXXX]
(Inner periphery: 0-100000h, Outer periphery: 180000-230000h)
Error rate [Err:X.XXE-X]
Rotation ratio display of the drive (/: Normal speed, No display: Double speed)
Command execution time ([Tn: XXXXns]
(Normally, double speed playback is 60ms degree in the internal periphery and it is 50ms degree in the outer periphery.)
* When normal playback and command execution time are long, problem occurs in performance of readout from the disc.
(Crack and dirt of the disc, and pickup of the drive is dirty, etc..)

● Subscreen 2– 4 (These menus are for design use.)

8. Mode Menu 8 [ATA/ATAPI-related debug display]

● Subscreen 1– 2 (These menus are for design use.)

● Subscreen 3

	ATA/ATAPI	WRITER	&	Vmecha	&	FAN
①	power ON	00	00	00	0000	0000000
	00000106	01	00	00	0000	0000000
②	Laser ON	02	00	00	0000	0000000
	00000142	03	00	00	0000	0000000
③	Recording	04	00	00	0000	0000000
	0000000A	05	00	00	0000	0000000
④	FAN:OFF	06	00	00	0000	0000000
⑤	TEMP:CB	07	00	00	0000	0000000
⑥	00000050 - 00000348					

- ① Power ON time of the drive (HEX display) [XXXXXXXXXhour]
② Laser ON time except during record (playback) (HEX display) [XXXXXXXXXhour]
③ Recording time (HEX display) [XXXXXXXXXhour]
④ Active state of the Fan for drive (ON/OFF)
⑤ Temperature in the drive [XX] (CB: 45°C, One count: Convert it with $\pm 1.6^{\circ}\text{C}$)
⑥ Fan ON time - Fan OFF time (HEX display) [XXXXXXXXX-XXXXXXXXXsecond]
* ①-③ data is stored even if power turned off.

9. Mode Menu 9 [GUI-related debug display]

● Subscreen 1– 2 (These menus are for design use.)

10. Mode Menu 10 [DVD VIDEO playback-related debug display]

● Subscreen 1– 10 (These menus are for design use.)

These subscreens have been exported from the debugging displays of the DV-737. For details on display content, refer to the service manual for DV-737 (Order No. RRV2320).

11. Mode Menu 11 [DVD VIDEO key processing history display]

● Subscreen 1 (This menu is for design use.)

Error Message	Description
Tr : NullBlk	Transfer task: NULL at the top block (Detecting NG stream made at the DVR-1000 series and starting protection process.)
Tr : ReadErr	Transfer task: ATA read error
Tr : SchLate	Transfer task: ATA search late
Tr : SemTOvr	Transfer task: Timeout for gaining semaphore (no synchronization with the display)
Tr : NaviErr	Transfer task: Inconsistency between NAVI (navigator) of management data and actual NAVI
Tr : OrderEr	Transfer task: Inconsistent order
Mn : Av1Hang	Main task: Detects hang-up of AV decoder and starts recovery
ERR_RCV!	TPP task: Detects hang-up of AV decoder and starts recovery
Tp : VobDif+	TPP task: The decoder STC advances by 1 VOB hour.
Tp : VobDif-	TPP task: The STC of the management information advances
Tp : midNULL	TPP task: The management information pointer designated was NULL.
Tp : ScanNg	TPP task: Failure to set the TPP memory when scanning was canceled.
Tp : RStepEr	TPP task: Although the reverse step had failed, the operation was forcibly terminated because the top cell was located.
Tp : tppErr	TPP task: Inconsistency occurred.
Rv : 1stTOvr	Reverse playback task: Timeout for waiting for interruption to the top VOB immediately after starting decoding
Rv : OpnTOvr	Reverse playback task: Timeout for waiting for B-picture of the open GOP immediately after starting decoding
Rv : OplTOvr	Reverse playback task: Timeout for waiting for I-picture of the open GOP immediately after starting decoding
Rv : LnkTOvr	Reverse playback task: Timeout for waiting for link
Rv : LnkFail	Reverse playback task: Starts compensation by detecting link failure
Rv : R2FTOvr	Reverse playback task: Starts retrial after detecting timeout from reverse pause to forward pause
Rv : TopVbEr	Reverse playback task: Forced termination because of a possible error of the top data during reverse normal playback
Rv : OrderEr	Reverse playback task: Inconsistent order
Av : B/CTOvr	AV1: Buffer-clear timeout
Av : StrmOvr	AV1: Timeout for waiting for stream ready
Av : TpmTOvr	AV1: Timeout for TP mode change
Av : SpmTOvr	AV1: Timeout for a step command
CC_OS_ERR	Closed caption task: OS error
DAC_NG	Number of retrial for DAC setting is over.
DAC_Error	Failure to DAC setting

Table 7.1 Description of VR playback-related errors

[REFERENCE]

STC=System Time Clock , VOB=Video Object Unit , GOP=Group Of Picture , B-picture= Bidirectionally predictive-picture
I-picture=Intra-picture, P-picture=Predictive-pictute, TP mode change=AV1 term (Trick Play mode change)

Error Message	Description	Error Message	Description
Non Err	Normal	No Video	No video input (not locked)
DRAM NG	Abnormality in access to the DRAM for work	Invalid Param	Invalid parameter
SRAM NG	Abnormality in access to the backup SRAM for work	Protect Src	Source to be recorded is write-protected.
CPRM IC NG	Inappropriate CPRM IC	Now Busy	In the process of the emergency processing
Drive Destroy	The drive was destroyed.	Invalid Disc	The disc cannot be recognized.
MKB REVOKED	Error in gaining data	Invalid UDF	Invalid UDF content
BK BATT Down	Backup RAM data has been erased.	Invalid VMG	Invalid VMG content
BK FSYS Dirty	Backup RAM data has not been written on the file system.	Invalid TMVMG	Invalid TMP_VMG content
Stream NG	Inappropriate input stream data	Unmatch Stamp	Impossible to modify because of unmatched time stamps
Stm Start NG	Failure to start encoding (reasons not clear)	Virgin DISC	Blank disc
Excel Hang	Dvexcel NG was announced.	Fail Repair	Repair failed.
No SysHdr IN	System packet is not input periodically.	ReadOnly DISC	Because part of data is invalid, data cannot be written.
Strm Start NG	Timeout of system packet input at the beginning	Rzn Rsv NG	R Zone Reserve failed.
IN Encode	Changes cannot be made in the process of encoding.	Rzn Cls NG	R Zone Close failed.
EncModul Hang	Encoder routine is hung up.	Rzn Rpr NG	R Zone Repair failed.
Ourob Strm NG	Inappropriate stream data to the Ouroboros input	Bdr Opn	Open Border failed.
BUF Overflow	Overflow of stream buffer	Bdr Cls	Close Border failed.
Drive Hang	Drive is hung up.	Format NG	Formatting failed.
Write Err	The drive failed to write and could not be recovered.	OPC NG	OPC failed.
Read Err	Reading failed, ECC failed, etc.	PCA Full	PCA has been used up.
Drv Hard Err	Abnormality in the drive hardware or firmware	RMA Full	RMA has been used up.
Mech No Res	No response from the mechanical U-Com	SW Vrec mode	Switching to video recording routine is required.
Drv TimeOut	Timeout for drive operation	SW Vpb mode	Switching to video playback routine is required.
NWA Exhaust	NWA surpassed and impossible to be used	Something	Something is wrong.
MKB Invalid	MKB reading error	Status NG	Abnormality in change of statuses
Drv Err	General error of the drive	Irr Action	Incorrect action
DISC Full	No further data can be written because the disc is full.	Abort	Cancellation
No More Info	No more space in the internal work management area	I am Down	A request to turn off the power was placed.
No Perm	No permission to write to the disc	Repair Exec	Repairing has been executed.
Limit Over	Standard maximum limit was over.	Format Exec	Formatting has been executed.
Rec Pause	No operation permitted during recording pause	BUG	Some bugs

Table 7.2 Description of VR recording-related errors

Note :

* A dark halftone dot meshing part is an error of the MPEG Encoder, and a light halftone dot meshing part is an error of the drive system.

* When the drive system is errored, there is a problem in crack and dirt of the disc or drive oneself (pickup is dirty).

[REFERENCE]

ECC=4 Byte code for error correction ,

UDF=Universal Disc Format ,

PCA= Power Calibration Area ,

OPC=Optical Power Control

NWA=Next Writable Address ,

VMG=Video Manager ,

RMA=Recording Management Area ,

MKB= Media Key Block ,

TMP_VMG=Temp Video Manager Information,

Border=from Lead-in to Lead-out ,

DVR-7000

7.1.4 SERVICE MODE

1. Error Rate Measurement

- How to Enter this Mode : Press the **[ESC]** and **[SIDE-B]** buttons sequentially.

Functions : When enter this mode, measure the error rate automatically.

- ① VR mode record
Record it for 10 seconds and playback the title.
During the playback and stop, display the error rate in FL and OSD.
ERR RATE : *.**E-*
- ② Video mode record
Record it for 30 seconds and playback the title.
During the playback and stop, display the error rate in FL and OSD.
ER (av):*. *E- * * (Display - during measurements)
- ③ DVD-VIDEO playback
Playback, and measure the error rate and display it. Stop afterwards.
ER (av):*. *e- * * (Display - during measurements)
- ④ CD
Trace it from the lead of track 1 and display the error rate.
E. RATE:*. *e-*

- How to Release : Press the **[ESC]** button to release from this mode.

2. Error Rate Measurement During DVD-VIDEO Playback

- How to Enter this Mode : Press the **[ESC]** and **[n]** buttons sequentially during playback. (n: Numeric button)

Functions : When enter this mode, measure the error rate of DVD-VIDEO and display it.

Record it for 10 seconds and playback the title.

ER (av):*. *e- * * (Display - during measurements)

- How to Release: Press the **[ESC]** button to release from this mode.

3. VR Aging Mode

- How to Enter this Mode : Press the **[ESC]** and **[REP.B]** buttons sequentially to enter the aging mode.
Display **[AGING]** on the left part of FL and display loop count on the right part of FL during this mode.

Functions : When enter this mode, repeat the following operations automatically.

- ① VR initialization
 - ② Video recording 60 minutes
 - ③ Playback 45 minutes
 - ④ Tray open
 - ⑤ Tray close
- Display the following counts in FL during the aging mode.
[AGING 0001]

- How to Release : Press the **[ESC]** button to release from this mode.

Note : Aging Mode stops when an error occurs. Press the **[ESC]** button to release from this mode.

And see the error history with Debugging Mode.

4. Version Display

- How to Enter this Mode : Press the **[ESC]** and **[FRM/TIM]** buttons sequentially to display the version information screen.

- How to Release : Press the **[ESC]** button to release from this mode. (screen disappears)

5. Version Display (for Remote Control Unit of Accessory)

- How to Enter this Mode : Perform highlight display the position of "main unit setting / voice output / digital output / ON", and press the **[ANGLE]** button of the remote control unit of accessory.

The following display appears at a position of the third layer.

```
SYSCON : RELEASE_112
TUFLCON : 1.5200 *
DRIVE : 1.61C *
DEVICE : AV1=ES6.0
```

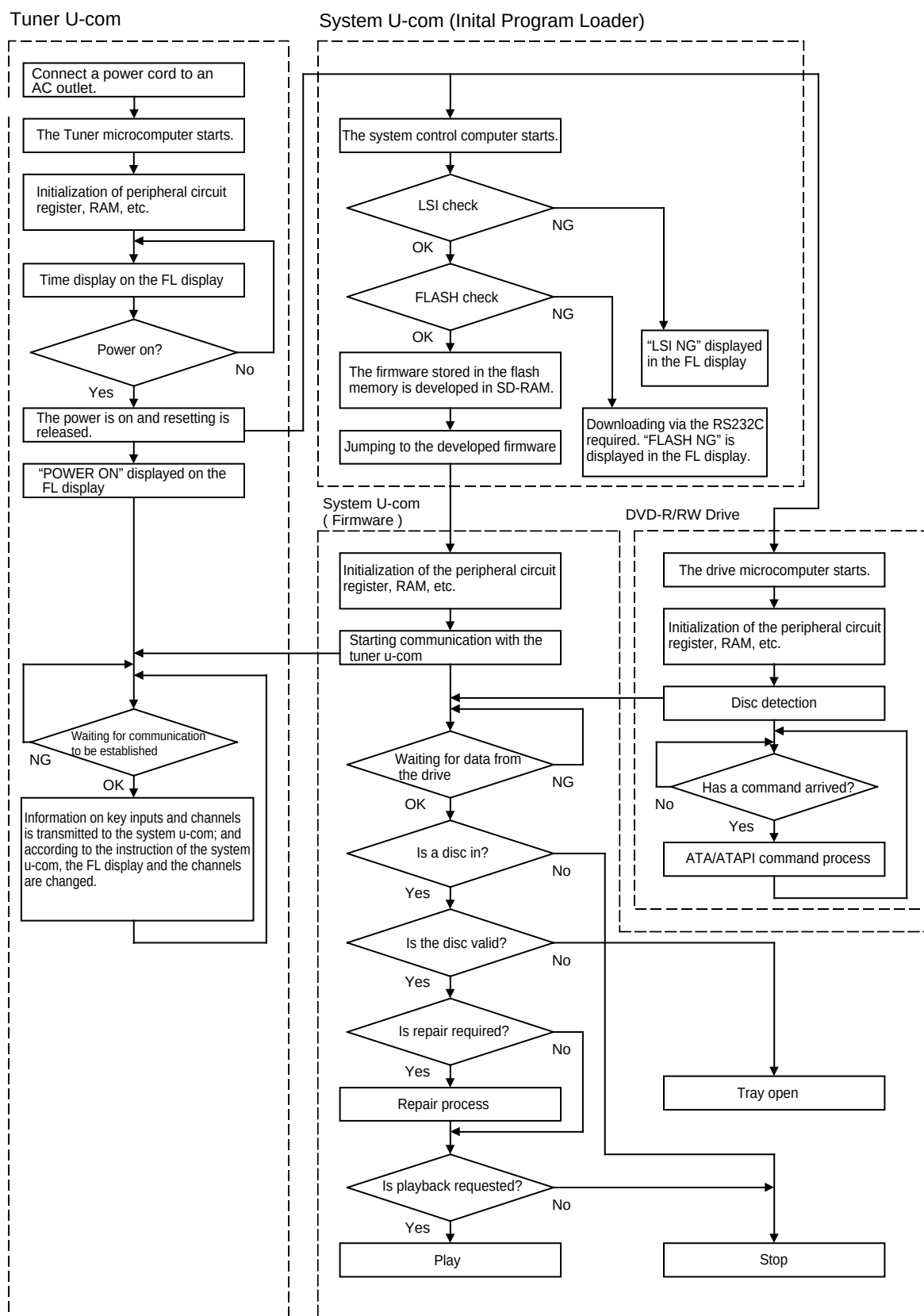
6. FL All Lighting Mode

- How to Enter this Mode : All FL lights when pressing the **[ESC]** and **[TEST]** buttons sequentially.

- How to Release : Press the **[ESC]** button to release from this mode. (Return to normal display.)

Note : Take care not to light all FL Tube for long time.

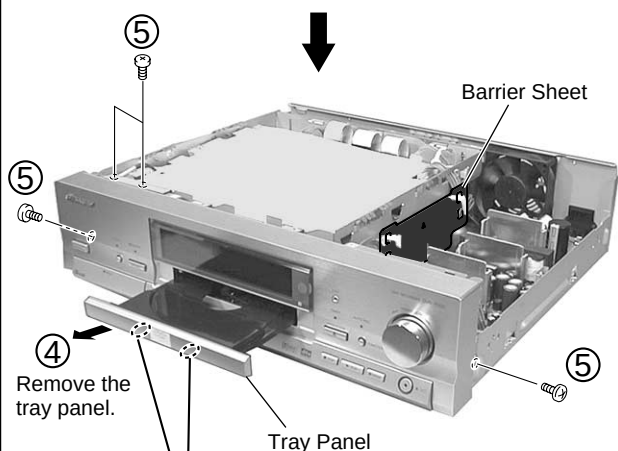
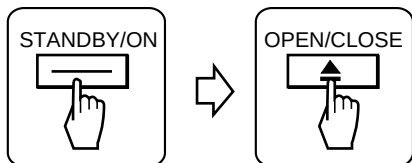
7.1.5 POWER ON SEQUENCE



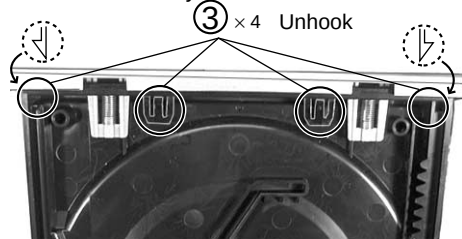
7.1.6 DISASSEMBLY

① Remove the bonnet. (Screw ×10)

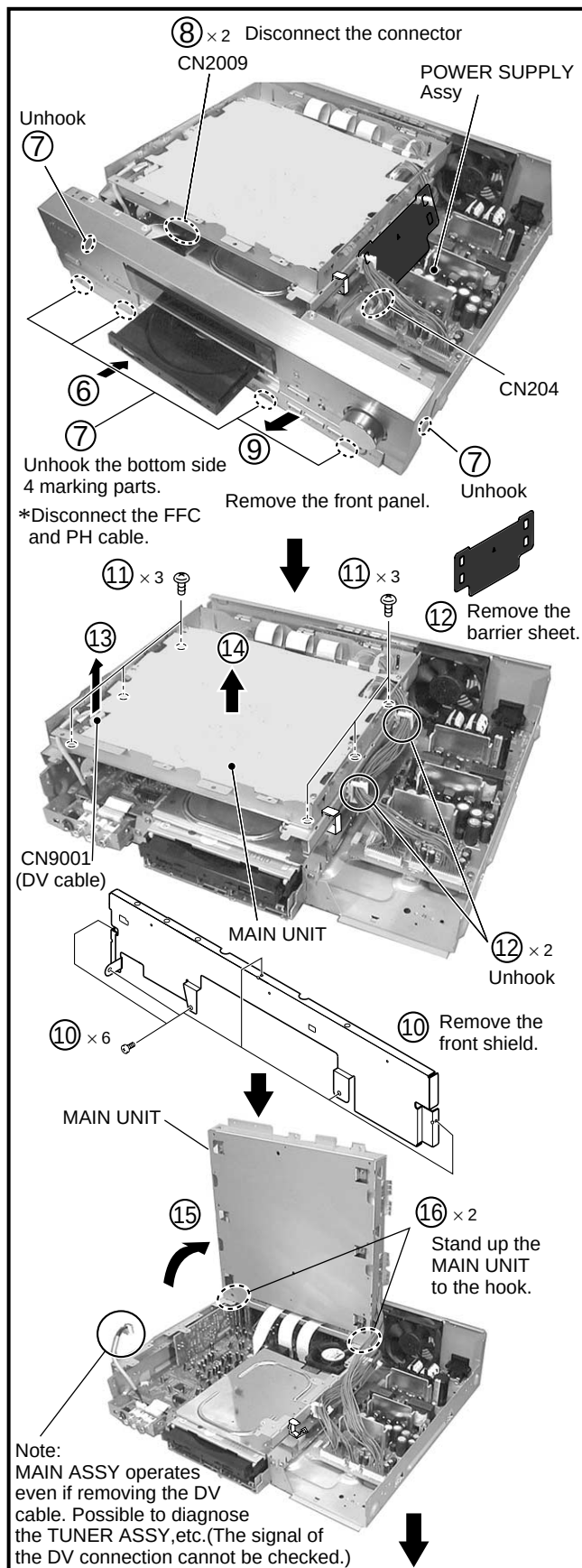
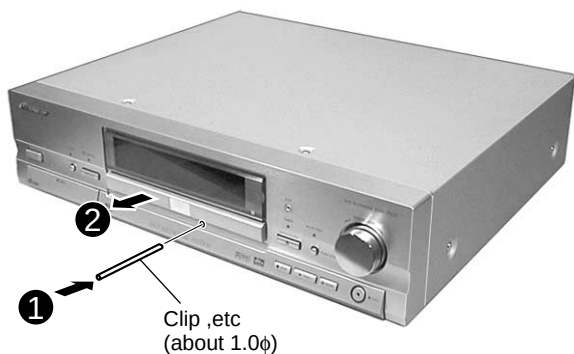
② Open the tray.



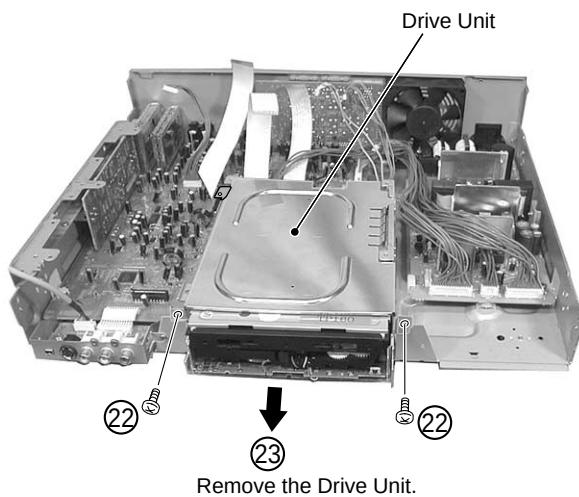
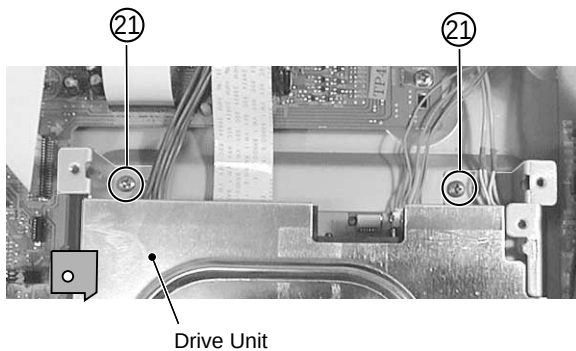
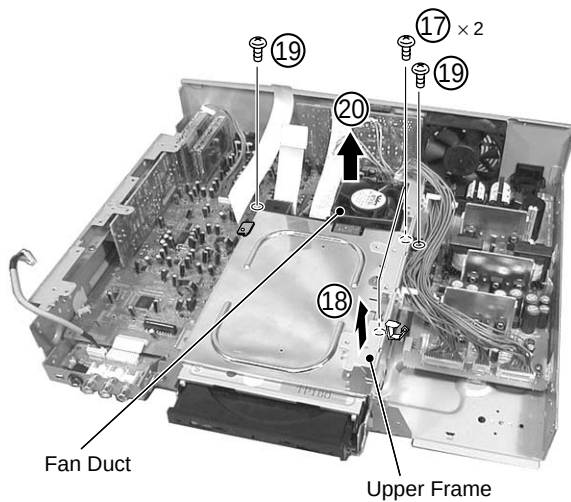
●Rear side of the tray



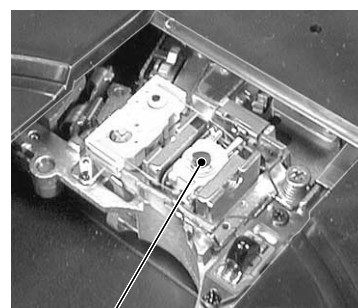
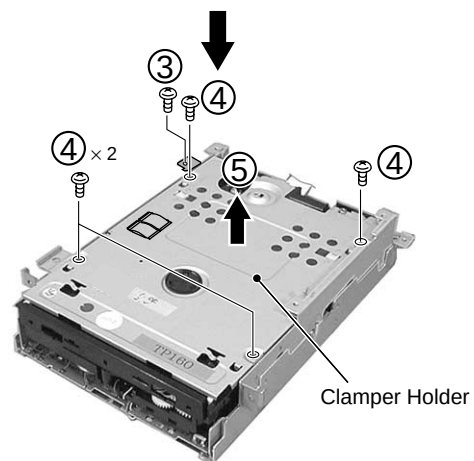
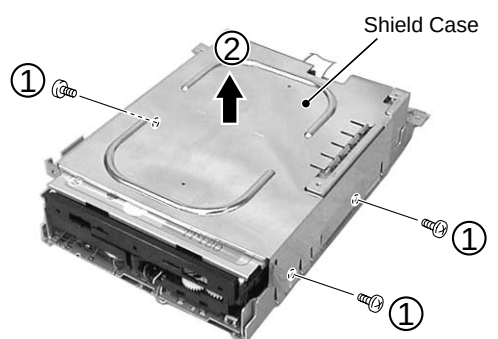
●When opening the tray by manual operation



⑬ Disconnect all connectors on the MAIN ASSY. (×7)

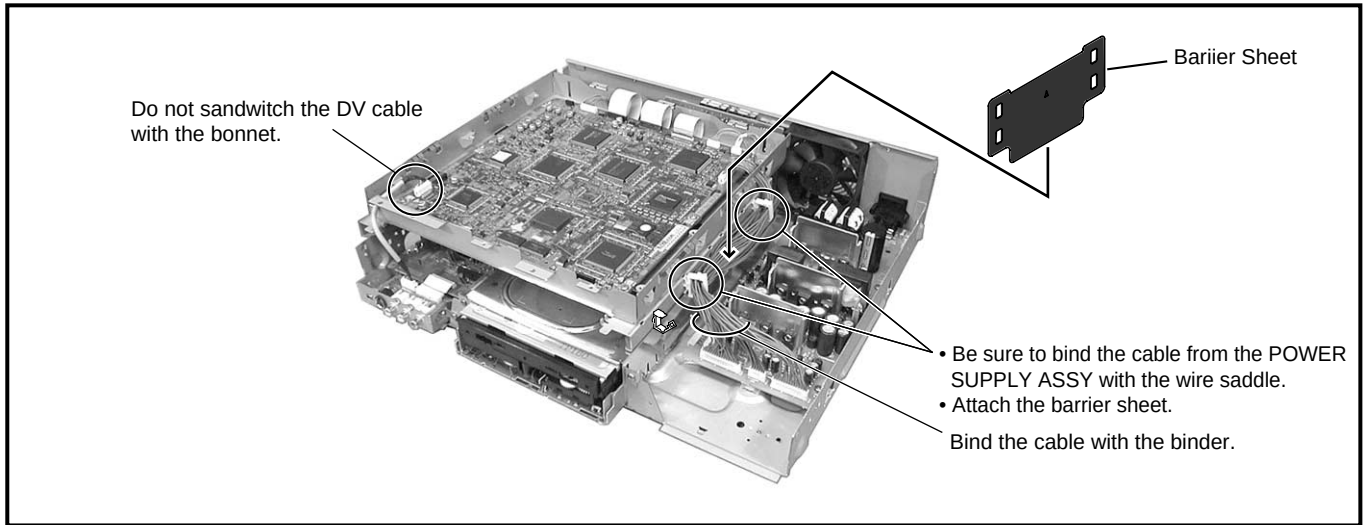


■ DRIVE UNIT

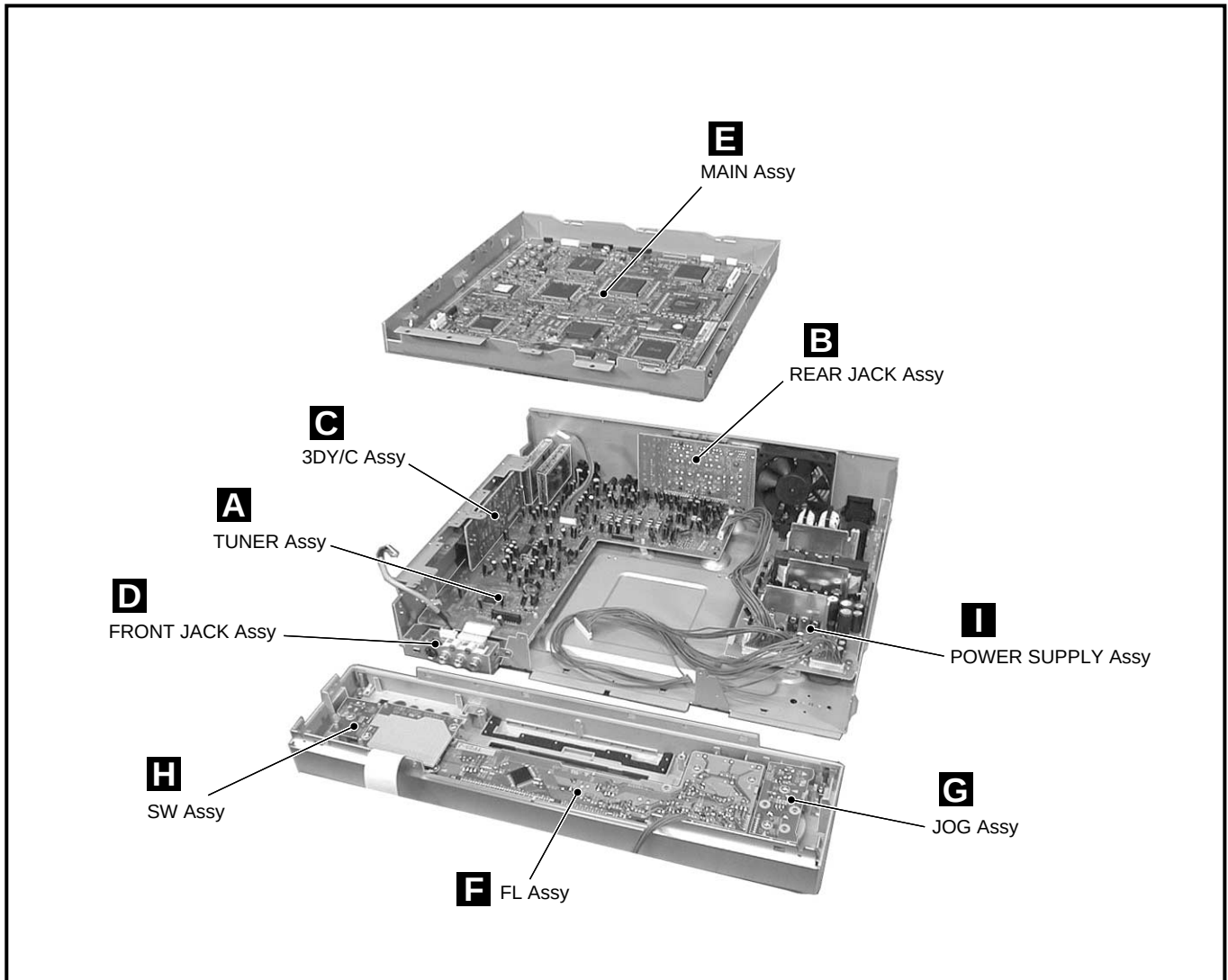


⑥ Make clean the pick-up lens.

■ CAUTION FOR CABLE STYLING



■ PCB BOARD LOCATION



7.2 IC

• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

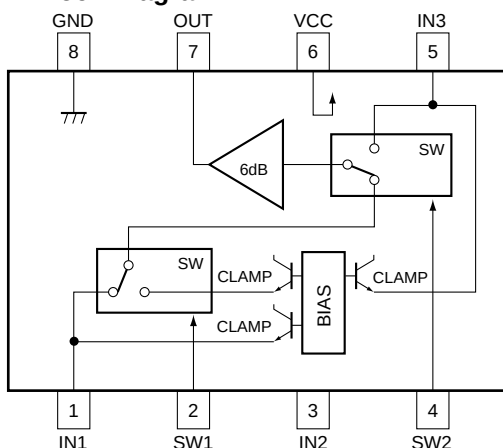
• List of IC

MM1118XF, TK15452V, TK15453V, BA7665FS, PE5275, RV5C386A, CXA2094Q, LC7454M, HD6417709AF100B, PE5219A, PD6342A, DVXCEL-BA1, UPD61003, PE7004A, CS8420-CS, TC9412AF, PD0272A, TSB42AB4PDT, TSB41AB2PAP, PE7003B, PDY078A, UPD65954-GC-E59-7EA

■ MM1118XF (TUJB ASSY : IC1003, IC1004, IC1171)

• Video Switch IC

• Block Diagram



• Truth Table

SW1	SW2	OUT
L	L	IN1
H	L	IN2
-	H	IN3

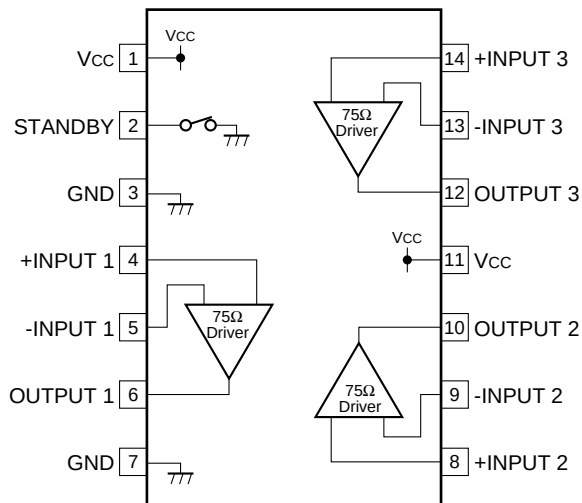
• Pin Function

No.	Pin Name	Function
1	IN1	Input (1)
2	SW1	Switch (1)
3	IN2	Input (2)
4	SW2	Switch (2)
5	IN3	Input (3)
6	Vcc	Power supply
7	OUT	Output
8	GND	Ground

■ TK15452V (TUJB ASSY : IC1311)

• Video Amplifier IC

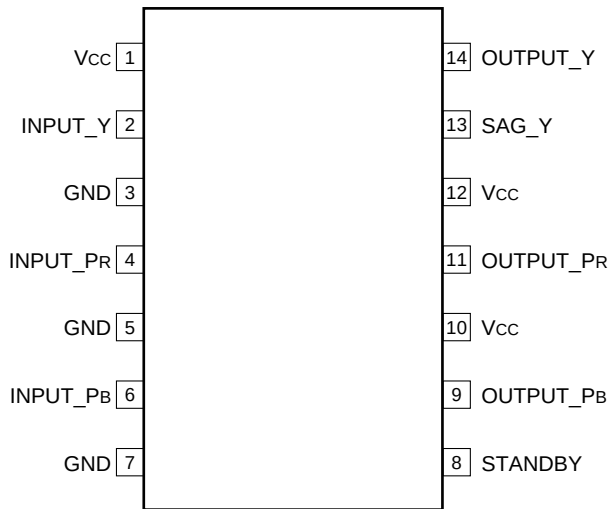
• Block Diagram



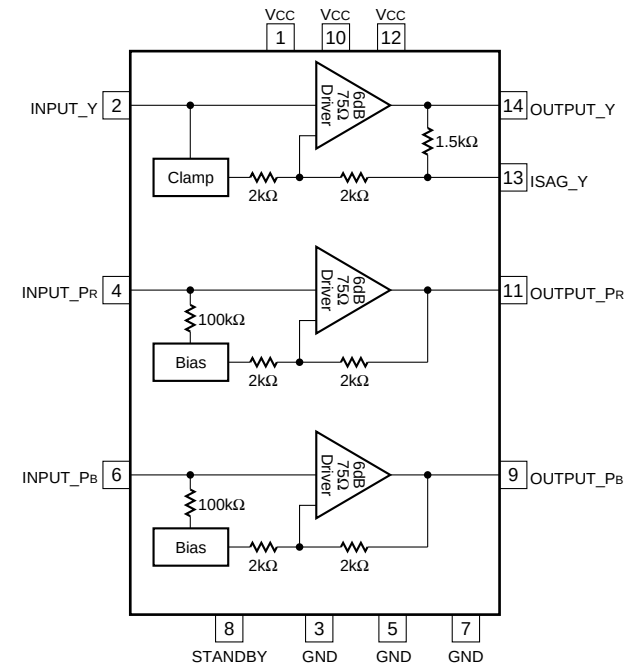
TK15453V (TUJB ASSY : IC1312)

• Video Amplifier IC

• Pin Assignment (Top view)



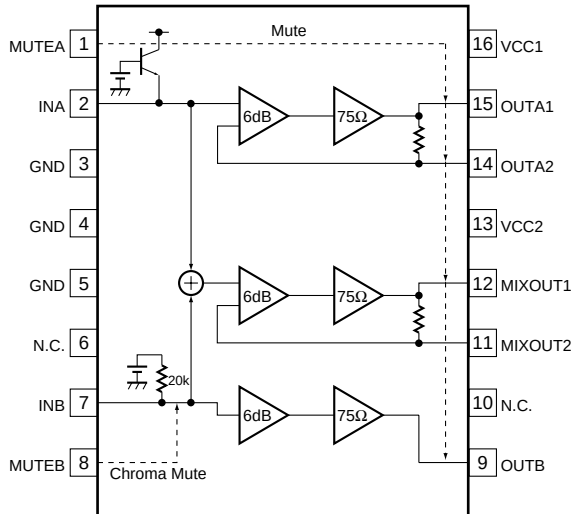
• Block Diagram



BA7665FS (TUJB ASSY : IC1351)

• Video IC

• Block Diagram



• Pin Function

No.	Pin Name	I/O	Pin Function
1	MUTEA	I	Mute control pin
2	INA	I	Composite Y signal input pin
3	GND	–	Ground
4	GND	–	Ground
5	GND	–	Ground
6	N.C.	–	Non connection
7	INB	I	Chroma signal input pin
8	MUTEB	I	Mute control pin
9	OUTB	O	Chroma signal output pin
10	N.C.	–	Non connection
11	MIXOUT2	O	Y/C MIX signal output pin
12	MIXOUT1	O	Y/C MIX signal output pin
13	VCC2	–	Power supply pin
14	OUTA2	O	Composite Y signal output pin
15	OUTA1	O	Composite Y signal output pin
16	VCC1	–	Power supply pin

PE5275 (TUJB ASSY : IC2003)

• Tuner Control Microcomputer

• Pin Function (1/2)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
1	P120	TIMER	O	LED for timer	41	P21	TXD1	O	MAIN communication line
2	P121	DVDLED	O	DVDLED	42	P22	ASCK1	I	
3	P122	FLOFF	O	For FL OFF	43	P23	TUREQ	O	Communication request of tuner control IC
4	P123	DOLBY	O	LED for FL DOLBY	44	P24	WRTPT	O	EEPROM writing permission
5	P124	FLCS	O	FL Driver communication line	45	P25	SDAM	I/O	I2C data input/output
6	P125	XFLRST	O	FL DRIVE reset signal	46	P26	XRESET	O	RESET OUT
7	P126	JOGA	I	FL JOG input	47	P27	SCLM	O	I2C clock input
8	P127	JOGB	I	FL JOG input	48	P80	IOC	O	Data input/output control signal of LC7454
9	VDD	VDD	–	Power supply	49	P81	SLICE	I	Pulse output at XDS specification line
10	X2	X2	I	Connect a 6MHz ceralock	50	P82	NC	–	NC
11	X1	X1			51	P83	P_ON	O	POWER ON signal
12	Vss	Vss	–	Ground	52	P84	NC	–	NC
13	XT2	XT2	I	32k input	53	P85	NC		
14	XT1	XT1			54	P86	NC	–	NC
15	XRESET	XRESETIN	I	Reset IC input	55	P87	TUSEL1	O	Select the ground wave or BS
16	P00	TUACK	I	MAIN communication line	56	P40	TUSEL2		
17	P01	XINTRA	I	RTC communication	57	P41	GOSTCS	O	Gauguin peripheral chip select
18	P02	XINTB			58	P42	XCVBS	O	S composite select
19	P03	NC	–	NC	59	P43	XTUMTE	O	Video mute at input switch to George
20	P04	NSTD	I	3-dimensional non-standard detection	60	P44	X3D	O	3-dimensional Y/C select
21	P05	LN26	I	Both fields are 32 μ pulses with 26 LINE	61	P45	LINSEL1	O	External input switch 1
22	P06	NC	–	NC	62	P46	LINSEL2	O	External input switch 2
23	AVdd	AVdd	–	Power supply	63	P47	F_ON	O	ON/OFF signal for fan
24	AVRef0	A/D Ref	I	A/D reference voltage input	64	P50	BUSY	I	Braster BUSY signal
25	P10	KEY1	I	FL KEY input 1	65	P51	XDSCE	O	XDS chip enable
26	P11	KEY2		FL KEY input 2	66	P52	XDSCK	O	XDS clock
27	P12	SONYKEY1	I	Front panel key for SONY	67	P53	FANDET	I	FAN rotation detection
28	P13	SONYKEY2			68	P54	TUON	O	Tuner ON
29	P14	NC	–	NC	69	P55	N3D	O	Forced 2D mode signal for three dimensions
30	P15	AFT	I	Ground wave tuning gap input	70	P56	SQUEEZE	O	SQUEEZE signal for D terminal and skirt
31	P16	THERMO	I	Temperature detection input	71	P57	LET_S	O	LETTER signal for S terminal
32	P17	NC	–	NC	72	Vss	Vss	–	Ground
33	Avss	Avss	–	Analog ground	73	P60	OECFO	I	Field distinction pulse output H: Odd numbers
34	P130	VI_ON	O	Video circuit ON for LINE input	74	P61	CPDT	I	XDS data output
35	P131	RSTCTL	O	Reset mute signal for sag measures	75	P62	BLCS	O	Chip select signal for braster
36	AVRef1	D/A Ref	I	D/A reference voltage input	76	P63	REGION1	I	Region 1
37	P70				77	P64	REGION2		Region 2
38	P71	FLDATA	O	FL DRIVER communication line	78	P65	AV1RST	O	AV1 reset signal
39	P72	FLCP			79	P66	XBRLST	O	Braster reset signal
40	P20	RXD1	I	MAIN communication line	80	P67	XSELCS	I	For S input detection/for S signal switch (EU)

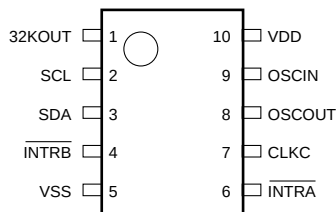
● Pin Function (2/2)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
81	VDD	VDD	–	Power supply	91	P35	SELIR	I	Remote control input
82	P100				92	P36			
83	P101				93	P37	XCHEKR	I	Checker mode
84	P102				94	TEST	VPP	I	VPP input for FLASH
85	P103				95	P90	MAKER1	I	Manufacture identification code 1
86	P30				96	P91	FLDIM1	O	For FLDIMER
87	P31				97	P92	FLDIM2		
88	P32				98	P93	REGION3	I	Destination code 3
89	P33				99	P94	MAKER2	I	Manufacture identification code 2
90	P34	CSSYNC	I	CSSYNC input for CSREC	100	P95	XSRVICE	I	Service mode

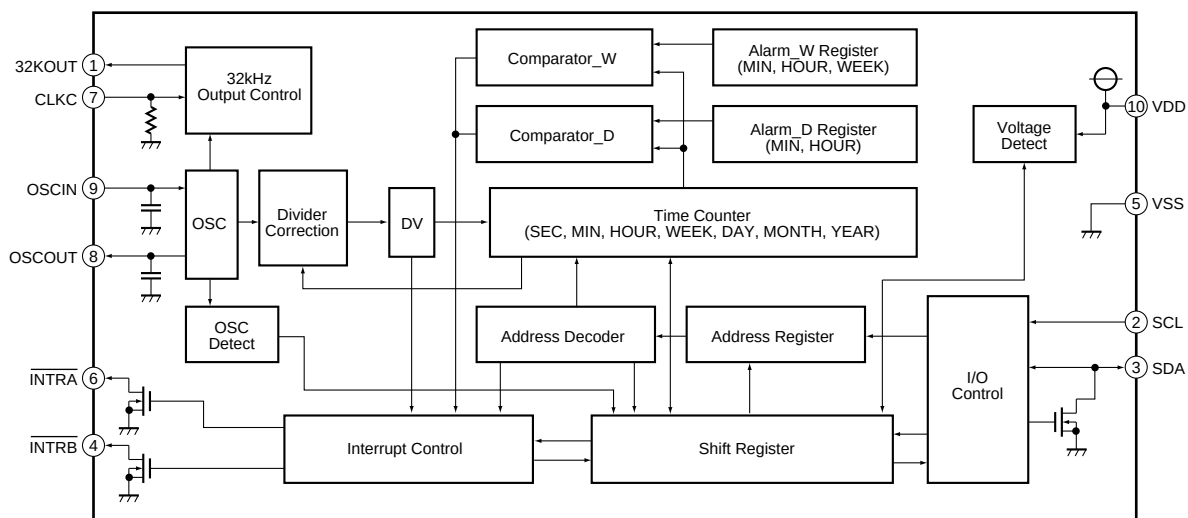
RV5C386A (TUJB ASSY : IC2008)

• Real Time Clock IC

• Pin Assignment (Top view)



• Block Diagram



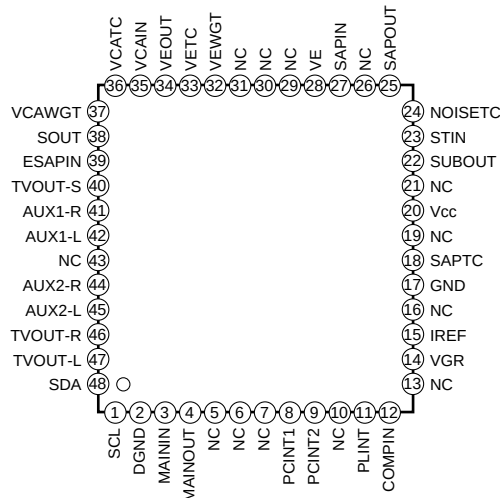
• Pin Function

No.	Pin Name	I/O	Pin Function
1	32KOUT	O	32.768kHz clock output When rises up the power supply from 0V, output a clock if CLKC terminal is "H". In the CMOS output, CLKC terminal does not output it at the time of "L" or open.
2	SCL	I	Serial clock input Synchronize with this clock, and input and output data from the SDA terminal. As for this input, input is possible to 5.5V without relation in power supply voltage.
3	SDA	I/O	Serial input and output Synchronize in SCL, and input and output the writing data or readout data. As for this input, input is possible to 5.5V without relation in power supply voltage. The output is open drain.
4	INTRB	O	Interrupt output B Output alarm interrupt (Alarm_W) for CPU. When rises up the power supply from 0V, it becomes off state. Nch open drain output.
5	VSS	-	Negative power supply input
6	INTRA	O	Interrupt output A Output alarm interrupt (Alarm_D) for CPU. When rises up the power supply from 0V, it becomes off state. Nch open drain output.
7	CLKC	I	Clock control input Control the 32KOUT output. At the time of "L" or open, 32KOUT output fixed to "L". Pull-down resistor is built in. As for this input, input is possible to 5.5V without relation in power supply voltage.
8	OSCOUT	O	Oscillation circuit output Connect a 32.768kHz crystal resonator.
9	OSCIN	I	Oscillation circuit input Connect a 32.768kHz crystal resonator.
10	VDD	-	Positive power supply input

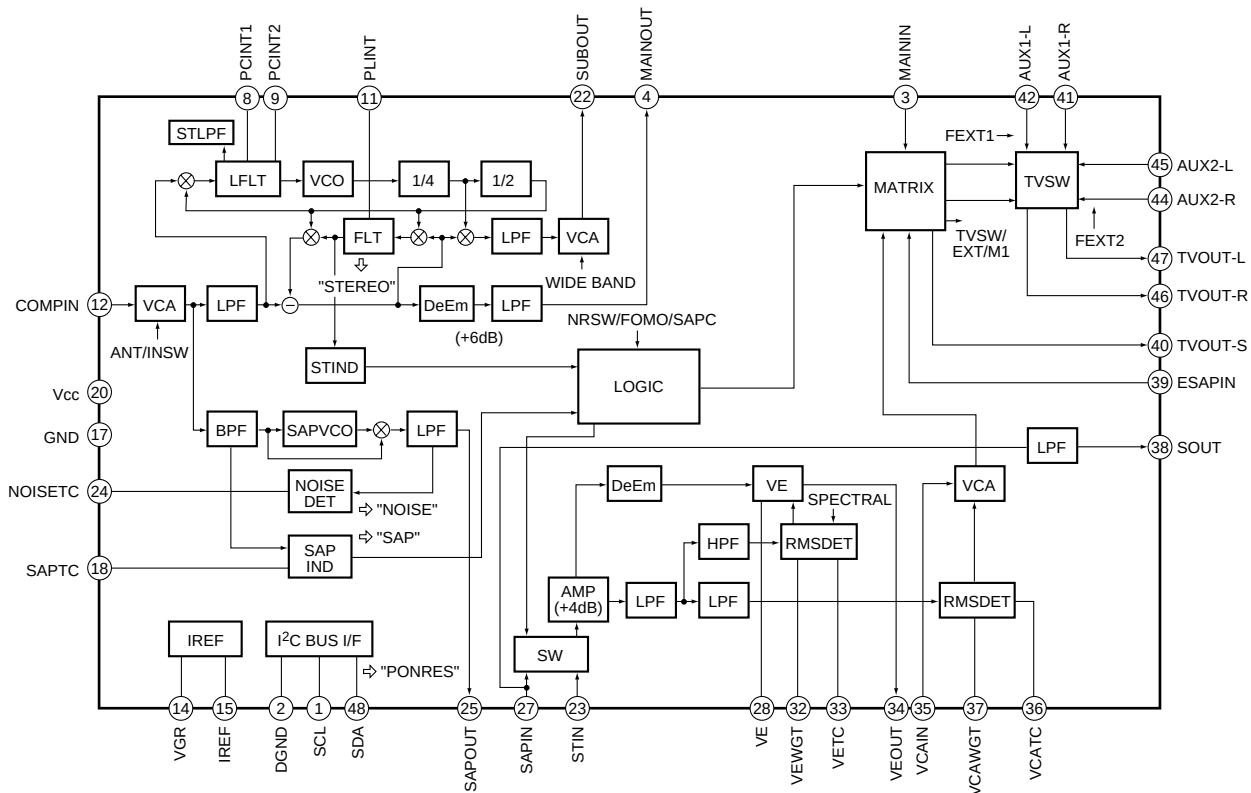
■ CXA2094Q (TUMJ ASSY : IC4601)

• Multi-channel Decoder IC

• Pin Assignment (Top view)



• Block Diagram



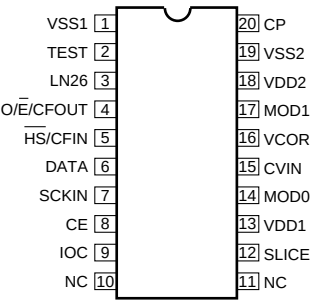
● Pin Function

No.	Pin Name	I/O	Pin Function
1	SCL	I	Serial clock input
2	DGND	–	Digital ground
3	MAININ	I	Inputs L+R signal from MAINOUT of pin 4
4	MAINOUT	O	L+R signal output
5	NC	–	NC
6	NC	–	NC
7	NC	–	NC
8	PCINT1	–	Integral pin of PLL loop filter on the stereo block
9	PCINT2	–	
10	NC	–	NC
11	PLINT	–	Integral pin of loop filter on the pilot cancel circuit
12	COMPIN	I	Multiplex signal input
13	NC	–	NC
14	VGR	O	Band gap reference output
15	IREF	–	Reference current setting pin for filter and VCO
16	NC	–	NC
17	GND	–	Analog ground
18	SAPTC	–	Time constant setting pin for SAP carrier detection circuit
19	NC	–	NC
20	Vcc	–	power supply
21	NC	–	NC
22	SUBOUT	O	L-R signal output
23	STIN	I	Inputs L-R signal from SUBOUT of pin 22
24	NOISETC	–	Time constant setting pin for NOISE detection circuit
25	SAPOUT	O	FM detector output of SAP
26	NC	–	NC
27	SAPIN	I	Inputs SAP signal from SAPOUT of pin 25
28	VE	–	Integral pin of variable deemphasis
29	NC	–	NC
30	NC	–	NC
31	NC	–	NC
32	VEWGT	–	Weight pin of effective-value detector circuit of variable deemphasis control
33	VETC	–	Pin to decide the return time-constant of effective-value detector circuit of variable deemphasis control
34	VEOUT	O	Variable deemphasis output
35	VCAIN	I	VCA input
36	VCATC	–	Pin to decide the return time-constant of effective-value detector circuit of VCA control
37	VCAWGT	–	Weight pin of effective-value detector circuit of VCA control
38	SOUT	O	Simple SAP output
39	ESAPIN	I	Inputs a signal from SOUT of pin 38
40	TVOUT-S	O	Rear output Outputs monaural or simple SAP
41	AUX1-R	I	R ch external input (1)
42	AUX1-L	I	L ch external input (1)
43	NC	–	NC
44	AUX2-R	I	R ch external input (2)
45	AUX2-L	I	L ch external input (2)
46	TVOUT-R	O	R ch output of TVOUT
47	TVOUT-L	O	L ch output of TVOUT
48	SDA	I/O	Serial data input/output

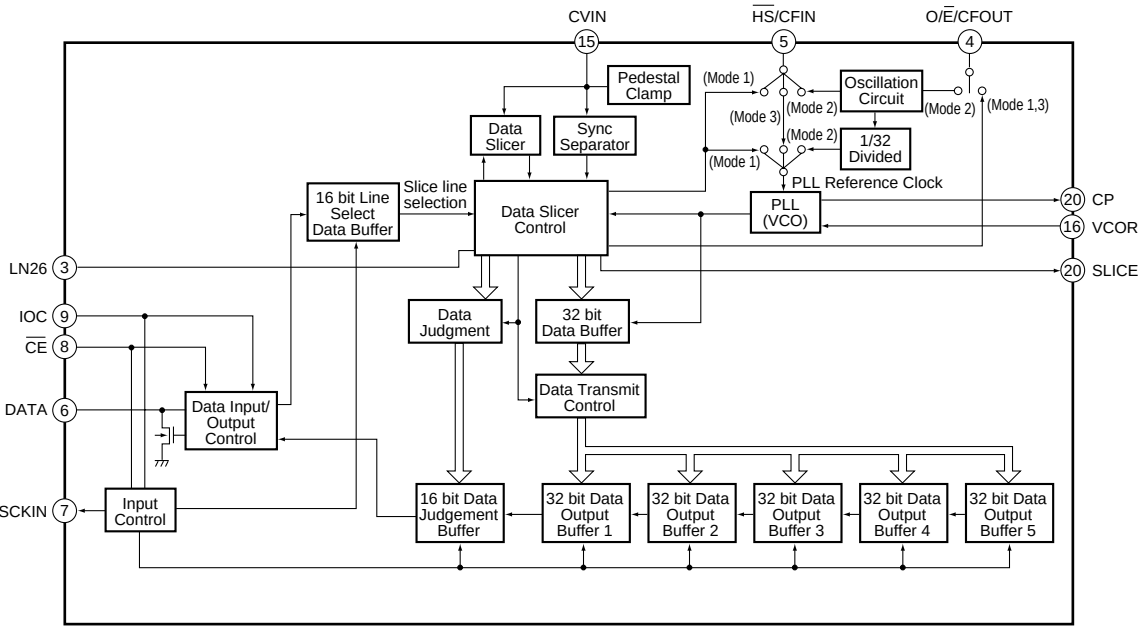
LC7454M (TUMJ ASSY : IC5001)

• CMOS Data Slicer

• Pin Assignment (Top view)



• Block Diagram



• Operation on Each Mode

The LC7454M has three operating modes. The operation mode can be selected by the status of MOD0 and MOD1 terminals. The functionality of three modes is the same. Only the PLL reference frequency which is used to generate the internal operation clock is different. Use model or mode3 only in the application which is used to generate the internal operation clock is different. Use model or mode3 only in the application which uses 2x data. Any mode (Mode1, 2 and 3) can be used in the 1x data only application.

Pin Name		Mode	Applications	PLL Reference
MOD1	MOD0			
Open	Open	Mode 1	NTSC-VCR	Use H-sync signal which is separated from C-Video signal.
Open	VDD	Mode 2	NTSC-VCR	Use 1/32 divided signal 503kHz which is generated by external ceramic resonator.
VDD	Open	Mode 3	NTSC-TV	Use H-sync signal from Fly Back.

● Pin Function

No.	Pin Name	Pin Function		
		Mode 1	Mode 2	Mode 3
1	VSS1	Ground		
2	TEST	Test pin, open in normal operation.		
3	LN26	32 μ s pulse output at line 26 timing on both field.		
4	O/XE/CFOUT	Pulse output for field judgment *1	Output pin for ceramic resonator	Pulse output for field judgment *1
5	XHS/CFIN	Sync separated XHS pulse output	Input pin for ceramic resonator	External XHS pulse input
6	DATA	Line select data input and slice data output *2		
7	SCKIN	Data transmit clock input		
8	XCE	Chip select input *3		
9	IOC	Data direction control signal input *4		
10	NC	NC		
11	NC	NC		
12	SLICE	Pulse output at selected slice line		
13	VDD1	Power supply		
14	MOD0	Open	Connect to VDD	Open
15	CVIN	Composite video input		
16	VCOR	Connect resistor for internal VCO oscillation frequency control		
17	MOD1	Open	Open	Connect to VDD
18	VDD2	Power supply		
19	VSS2	Ground		
20	CP	Filter pin for internal PLL		

*1: "H" level in Odd field, "L" level in Even field.

*2: N-ch open drain in output mode.

*3: For chip select input, apply the "L" level only when data transmission is in effect.

If CE="H", data terminal will be input/output disabled, and SCKIN terminal will be input disabled.

*4: "H" level : Output mode , "L" level : Input mode

■ HD6417709AF100B (MAIN ASSY : IC1010)

• MPU IC

● Pin Function (1/3)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
1	MD1	SHMD1	I	CLK mode setting	41	D9	D9	I/O	Data bus
2	MD2	SHMD2			42	D8	D8		
3	1.9V				43	D7	D7		
4	XTAL2	XTAL2	O	For RTC	44	D6	D6		
5	EXTAL2	EXTAL2	I		45	GND		–	Ground
6	GND (RTC)		–	Ground	46	D5	D5	I/O	Data bus
7	NMI	NMI	I	NMI interruption (Pull up)	47	VCCQ			
8	IRQ0	XIRQ0	I	AV1 interruption (Pull up)	48	D4	D4	I/O	Data bus
9	IRQ1	XIRQ1		Dvxccl interruption (Pull up)	49	D3	D3		
10	IRQ2	XIRQ2			50	D2	D2		
11	IRQ3	XIRQ3		Audery interruption (Pull up)	51	D1	D1		
12	IRQ4	XIRQ4		AV-1 (2nd) interruption	52	D0	D0		
13	D31	D31	I/O	Data bus	53	A0	A0	O	Address bus
14	D30	D30			54	A1	A1		
15	D29	D29			55	A2	A2		
16	D28	D28			56	A3	A3		
17	D27	D27			57	GND		–	Ground
18	D26	D26			58	A4	A4	O	Address bus
19	GND		–	Ground	59	VCCQ			
20	D25	D25	I/O	Data bus	60	A5	A5	O	Address bus
21	VCCQ				61	A6	A6		
22	D24	D24	I/O	Data bus	62	A7	A7		
23	D23	D23			63	A8	A8		
24	D22	D22			64	A9	A9		
25	D21	D21			65	A10	A10		
26	D20	D20			66	A11	A11		
27	GND		–	Ground	67	A12	A12	O	Address bus
28	D19	D19	I/O	Data bus	68	A13	A13		
29	1.9V				69	GND		–	Ground
30	D18	D18	I/O	Data bus	70	A14	A14	O	Address bus
31	D17	D17			71	VCCQ			
32	D16	D16			72	A15	A15	O	Address bus
33	GND		–	Ground	73	A16	A16		
34	D15	D15	I/O	Data bus	74	A17	A17		
35	VCCQ				75	A18	A18		
36	D14	D14	I/O	Data bus	76	A19	A19		
37	D13	D13			77	A20	A20		
38	D12	D12			78	A21	A21		
39	D11	D11			79	GND		–	Ground
40	D10	D10			80	A22	A22	O	Address bus

● Pin Function (2/3)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
81	1.9V				121	BACK		O	Not used (TP)
82	A23	A23	O	Address bus	122	BREQ		I	Not used (Pullup, TP)
83	GND		–	Ground	123	WAIT	XWAIT	I	Wait input (Pullup)
84	A24	A24	O	Address bus	124	RESETM	XRESET	I	Manual reset input (Pullup)
85	VCCQ				125	PTH5			(TP)
86	A25	A25	O	Address bus	126	PTG7			(TP)
87	BS	XBS	O	Bus cycle start signal	127	ASEMD0	ASEMD0	I	For H-UDI
88	RD	XRD	O	Read strobe	128	ASEBRKAK	ASEBRKAK	O	(AUD correspondence)
89	WE0	XWE0	O	Write strobe	129	PTG4			(TP)
90	WE1	XWE1			130	AUDATA3	AUDATA3	O	For H-UDI (AUD correspondence)
91	WE2	XWE2			131	AUDATA2	AUDATA2		
92	WE3	XWE3			132	GND		–	Ground
93	RD/WR	RDWR	O	Read / Write	133	AUDATA1	AUDATA1	O	For H-UDI (AUD correspondence)
94	AUDSYNC	AUDSYNC	O	For H-UDI (AUD correspondence)	134	1.9V			
95	GNDQ				135	AUDATA0	AUDATA0	O	For H-UDI (AUD correspondence)
96	CS0	XCS0	O	Chip select 0	136	TRST	TRST	I	For H-UDI (AUD correspondence) (pullup)
97	VCCQ				137	TMS	TMS		
98	CS2	XCS2	O	Chip select 2	138	TDI	TDI		
99	CS3	XCS3		Chip select 3	139	TCK	TCK		
100	CS4	XCS4		Chip select 4	140	PINT11	PINT11	I	Slalom interruption (Pullup)
101	CS5	XCS5		Chip select 5	141	PINT10	PINT10		(Pullup, TP)
102	CS6	XCS6		Chip select 6	142	PINT9	PINT9		WM interruption (Pullup)
103	PTE4	DVOEN	O	DV Req Mask	143	PINT8	PINT8		Slalom interruption (Pullup)
104	PTE5	SELVCD	O	Audio CLK switching control signal for V-CD	144	MD0	SHMD0	I	CLK mode setting
105	CKE	CKE	O	CKE for SDRAM	145	1.9V			
106	RAS3L	XRAS3L	O	RAS for SDRAM	146	CAP1	CAP1	–	For PLL
107	PTJ1		I/O		147	GND (PLL1)		–	Ground
108	CAS	XCASLL	O	CAS fro SDRAM	148	GND (PLL2)			
109	GNDQ				149	CAP2	CAP2	–	For PLL
110	PTJ3	XRSTPH	O	Reset output for 1394phy	150	1.9V			
111	VCCQ				151	AUDCK		O	For H-UDI (AUD correspondence)
112	PTJ4		I/O	I/O port for debugging (TP)	152	GND		–	Ground
113	PTJ5				153	GND			
114	DACK0	XDACK0	O	DMA ACK for Slalom/BY-chip	154	1.9V			
115	DACK1	XDACK1	O	DMA ACK for Vaikilt	155	XTAL	XTAL	O	CPU clock
116	PTE6	XRSTVQ	O	Reset output for VQE	156	EXTAL	EXTAL	I	CPU clock
117	PTE3	XDARST	O	Reset output for audio DAC	157	PTJ6	TUACK	O	Communication ACK signal of Tuner Control Microcomputer
118	PTE2	XRSTAU	O	Reset output for Audery	158	PTJ7	EDSEL	O	Bus switching signal for WM
119	PTE1	XRSTX	O	Reset output for DVxcel	159	TCLK		I/O	Clock I/O for TMU/RTC (TP)
120	TDO	TDO	O	For H-UDI (AUD correspondence)	160	IRQOUT		O	Not used (TP)

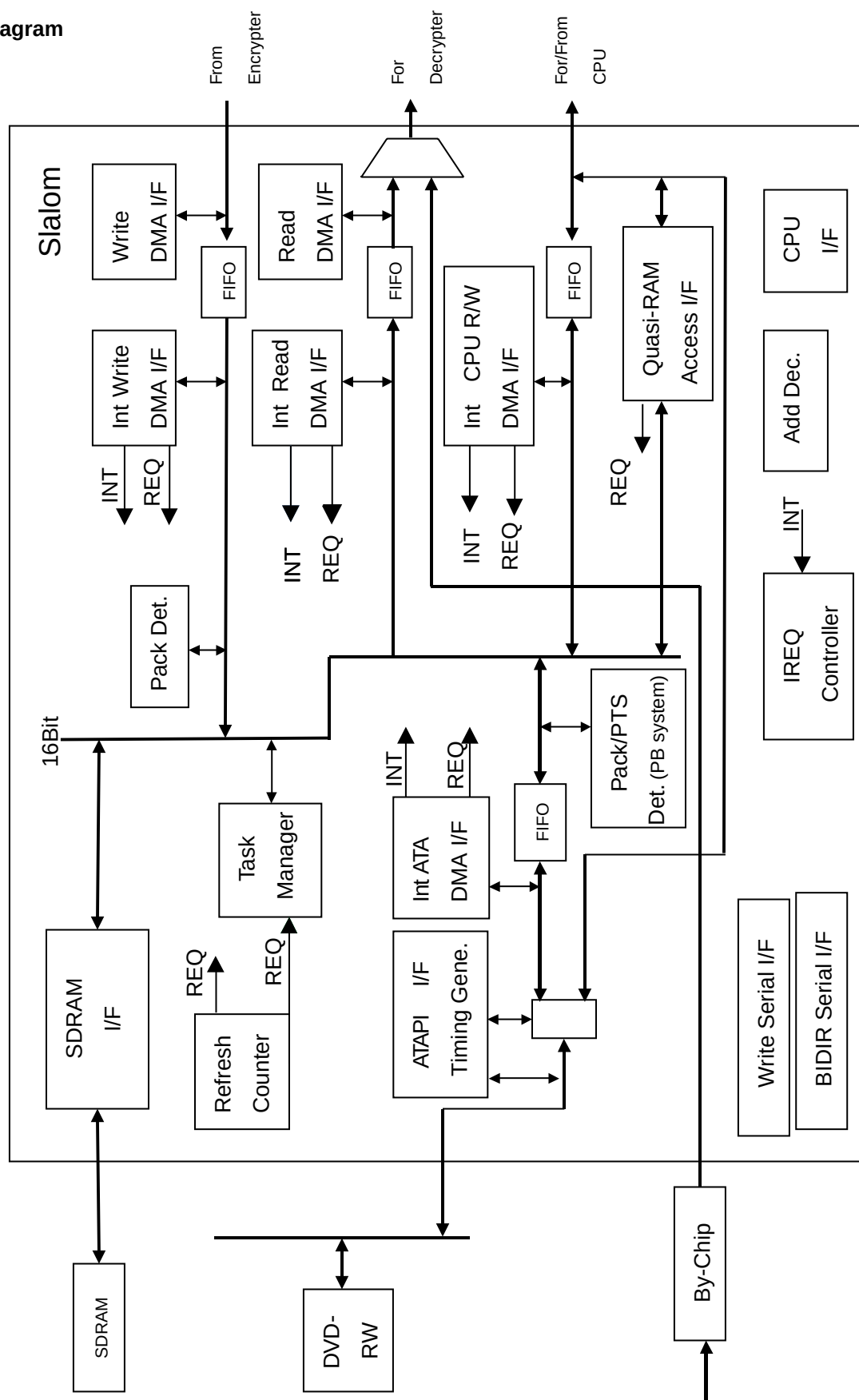
● Pin Function (3/3)

No.	Mark	Pin Name	I/O	Pin Function	No.	Mark	Pin Name	I/O	Pin Function
161	GND		–	Ground	185	PINT3	PINT3	I	1394celinx interruption
162	CKIO	CKIO	I/O	System clock I/O	186	PINT2	PINT2	I	Ouroboros interruption
163	VCCQ				187	PINT1	TUREQ	I	Tuner Control Microcomputer communication interruption
164	TXD0	TXD0	O	For Tuner Control Microcomputer	188	PINT0	PINT0	I	George VSYNC INT (Pull up)
165	SCK0	SCK0	O		189	PTD1		O	LED output for debugging
166	TXD1	TXD1	O	For RS232C	190	PTD0			
167	SCK1	SCK1	O	(TP)	191	DREQ0	DREQ0	I	DMA REQ for Slalom/By-chip
168	TXD2	TXD2	O	(For professional video)	192	DREQ1	DREQ1	I	DMA REQ for Vaikit
169	SCK2	SCK2	O	(TP)	193	RESETP	XRESETP	I	Power on reset input
170	RTS2	RTS2	O	(For professional video)	194	CA	CA	I	Chip active
171	RXD0	RXD0	O	For Tuner Control Microcomputer	195	MD3	SHMD3	I	Bus width setting for area 0
172	RXD1	RXD1	O	For RS232C	196	MD4	SHMD4		
173	GND		–	Ground	197	MD5	SHMD5	I	Endian setting
174	RXD2	RXD2	I	(For professional video)	198	AGND		–	Analog ground
175	1.9V				199	PTL0	DBP0	I	Audery DBP0
176	CTS2	XIRQ5	I	(For professional video)	200	PTL1	DBP1	I	Audery DBP1
177	PINT7	PINT7	I	By-chip interruption (Pull up)	201	PTL2	DBP2	I	Audery DBP2
178	PINT6	PINT6			202	PTL3	DBP3	I	Audery DBP3
179	PINT5	PINT5	I	Vaikilt interruption (Pull up)	203	PTL4	SRCPT	I	SRC lock signal
180	PINT4	PINT4			204	PTL5		I	(TP)
181	GND		–	Ground	205	AVCC			
182	PTD3		O	LED output for debugging	206	PTL6	VKGUI_T	I	(TP)
183	VCCQ				207	PTL7	DVLOCK	I	PLL lock judge signal for DV
184	PTD2		O	LED output for debugging	208	AGND		–	Analog ground

PE5219A (MAIN ASSY : IC3003)

• ATAP I/F LSI

• Block Diagram



● Pin Arrangement

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
1	GND	SHDATA 5	GND	SHDATA 0	GND	SHADD 21	SHADD 18	SHADD 15	SHADD 11	SHADD 8	SHADD 7	SHADD 3	SHWE1	SHCS5	SHCS2	SHDREQ	AVDREQ	AVDACK	AVDATA 5	AVDATA 2
2	CLK40M	SHDATA 8	SHDATA 6	SHDATA 3	SHADD 25	SHADD 22	SHADD 19	SHADD 16	SHADD 12	SHADD 10	SHADD 6	SHADD 2	SHWE0	SHCS4	GND	SHIRQS	TCK	AVDATA 4	TRST	CLK27M
3	SHDATA 12	SHDATA 7	GND	SHDATA 4	SHDATA 1	SHADD 23	SHADD 20	SHADD 17	SHADD 13	SHADD 9	SHADD 5	SHRD 1	SHRDWR	RST	SHIRQ	SHWAIT	AVDATA 7	AVDATA 3	GND	GND
4	SHDATA 13	SHDATA 11	SHDATA 10	GND	SHDATA 2	VDD	SHADD 24	GND	SHADD 14	VDD	SHADD 4	SHRD	GND	SHDACK	VDD	AVDATA 6	GND	AVDATA 1	AVDATA 0	DVDREQ
5	SDADD 3	SHDATA 14	VDD	SHDATA 9													CLK27 MO	TMS	DVDACK	TDI
6	SDADD 6	SDADD 5	SHDATA 15	VDD													VDD	TDO	DVDATA 6	DVDATA 5
7	GND	SDADD 1	SDADD 2	SDADD 4													DVDATA 7	DVDATA 4	VDD	DVDATA 3
8	SDADD 8	SDADD 0	SDADD 7	GND													GND	DVDATA 2	DVDATA 1	DVDATA 0
9	SDADD 11	SDADD 12	SDADD 9	SDADD 10													GND	CS2A0	CS21A	CS21B
10	CLK54 MO	GND	SDCS	SDADD 13													VDD	CS2A3	CS2A2	VDD
11	GND	SDRAS	SDCKE	VDD													CS4A3	CS4A2	CS4A1	CS4A0
12	SDCAS	SDWR	DQMU	DQML													CS5A6	CS5A5	CS5A2	GND
13	SDDATA 7	GND	SDDATA 8	GND													GND	VDD	NEWWE0	NEWWE1
14	SDDATA 6	SDDATA 9	SDDATA 5	SDDATA 11													SHBENB	GND	EXT WAIT3	NEWRD
15	SDDATA 10	SDDATA 4	SDDATA 3	VDD													VDD	SHDIR	EXT WAIT2	EXT WAIT0
16	SDDATA 2	SDDATA 12	VDD	SDDATA 1													TEST5	MCLK 27M	VDD	
17	SDDATA 13	SDDATA 0	SDDATA 15	GND	BYDATA 5	VDD	TIN	GND	ATAIRQ	VDD	VDD	ATA DATA6	GND	ATA DATA15	VDD	SR DATA0	GND	TEST6	TEST7	GND
18	SDDATA 14	CLK54M	BYDATA 1	BYDATA 6	BYCPU ACK	TEB	ATA IORDY	ATA IOWR	ATACS0	ATAADD 1	GND	ATA DATA5	ATA DATA9	ATA DATA11	ATA DATA14	SRCLK	VRCS	TEST1	TEST3	TEST8
19	GND	BYDATA 2	BYDATA 3	BYDATA 7	BYCPU REQ	ATAOE	ATA DACK	ATAIORD	ATACS1	ATAADD 2	ATA DATA2	ATA DATA4	ATA DATA8	ATA DATA10	ATA DATA13	ATARST	GND	VRDATA	TEST2	TEST4
20	BYDATA 0	BYDATA 4	BYDACK	BYDREQ	ATADIR	VDD	ATA DREQ	GND	ATAADD 0	ATA DATA0	ATA DATA1	ATA DATA3	ATA DATA7	GND	ATA DATA12	GND	SRCS	SR DATA1	VRCLK	TEST0

● Pin Function (1/2)

Pin Name	I/O	Function	Connection Point	Remarks
DQMU	O	Input mask / Output enable	SDRAM	
DVDATA	I	Data input	MPEG encoder	
DVDACK	O	DMA acknowledge	MPEG encoder	
DVDREQ	I	DMA request	MPEG encoder	
CLK27M	I	Clock input	Oscillation circuit	27MHz
CLK27MO	O	Clock output	MPEG encoder	27MHz
AVDATA	O	Data output	MPEG decoder	
AVDREQ	I	DMA request	MPEG decoder	
AVDACK	O	DMA acknowledge	MPEG decoder	
VRDATA	O	Data	Electric volume	
VRCLK	O	Clock output	Electric volume	
VRCS	O	Chip select/Data strobe	Electric volume	
SRDATAI	I	Data input	SRC	SRSSI
SRDATAO	O	Data output	SRC	SRSSO
SRCLK	O	Clock output	SRC	
SRCS	O	Chip select/Data strobe	SRC	SRXCS
EXTCS	O	Chip select	Peripheral device	CS2A0,
				CS21A,CS21B,
				CS2A3-2,CS4A3-0,
				CS5A2,CS5A6-5
NEWRD	O	Read	Peripheral device	
NEWWE	O	Write	Peripheral device	NEWWE1-0
EXTWAIT	I	Wait	Peripheral device	EXTWAIT3-0
SHBENB	O	Bus enable	Bus buffer	
SHDIR	O	Direction	Bus buffer	
MCLK27M	O	Clock output	George	27MHz
TEST	O	For TEST		TESTOUT8-0
TDI	I	JTAG		
TDO	O	JTAG		
TCK	I	JTAG		
TRST	1	JTAG		
TMS	I	JTAG		
TIN	I	For TEST	GND	
TEB	I	For TEST	VDD	

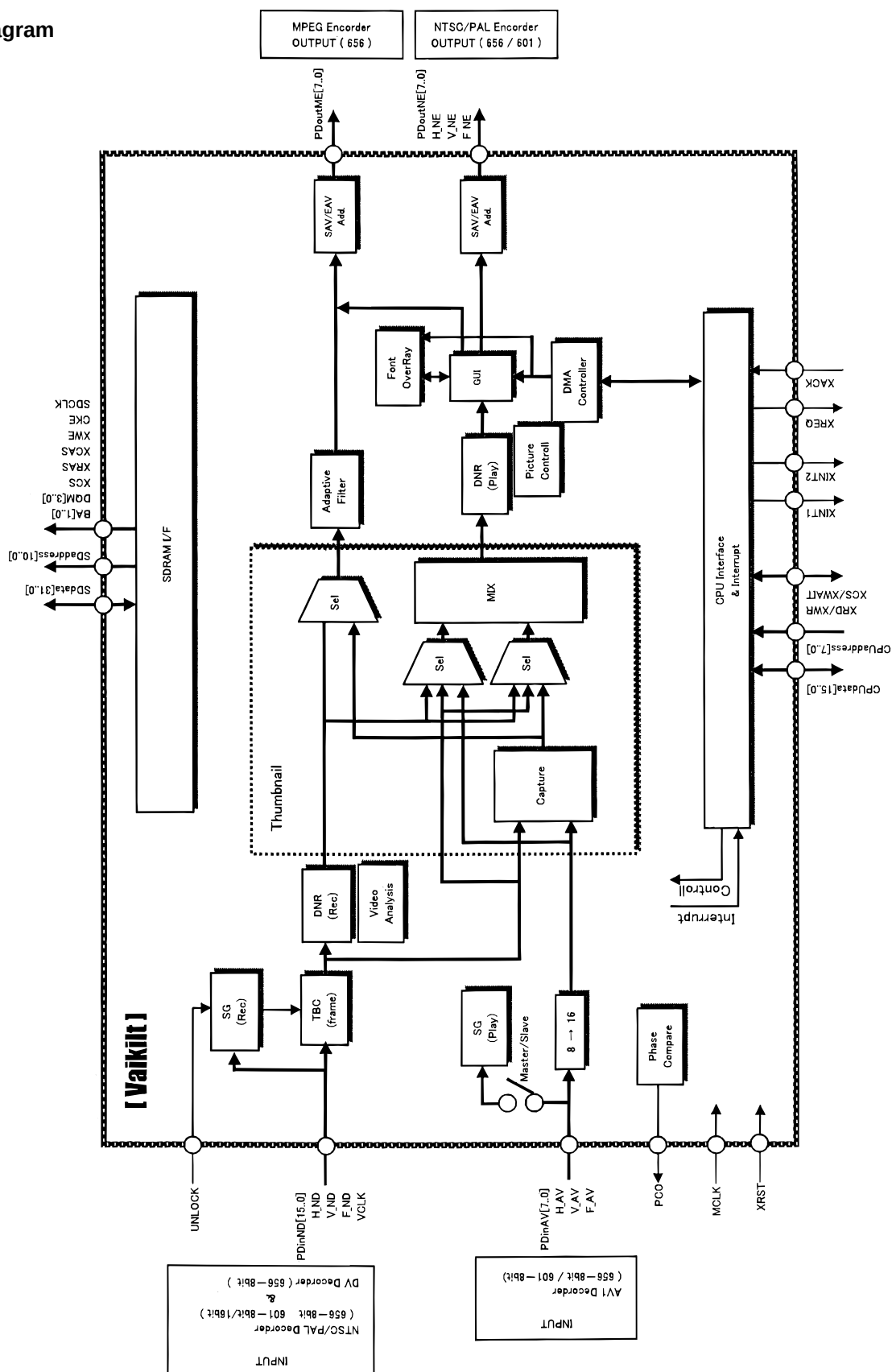
● Pin Function (2/2)

Pin Name	I/O	Function	Connection Point	Remarks
SHDATA	I/O	Data	CPU	
SHADD	I	Address	CPU	
SHRDWR	I	Read write	CPU	
SHRD	I	Read	CPU	
SHWE	I	Write	CPU	SHWE1-0
SHCS	I	Chip select	CPU	SHCS2,SHCS4,SHCS5
SHDREQ	O	DMA request	CPU	
SHDACK	I	DMA acknowledge	CPU	
SHIRQ	O	Interrupt	CPU	
SHIRQS	O	Interrupt	CPU	
SHWAIT	O	Wait	CPU	
RST	I	System reset	CPU	
CLK40M	I	Clock input	Oscillation circuit	40MHz (66MHz)
ATARST	O	ATA reset	ATA device	
ATADATA	I/O	Data	ATA device	
ATAADD	O	Address	ATA device	
ATACS	O	Chip select	ATA device	
ATAIRQ	I	Interrupt	ATA device	
ATAIORD	O	Read	ATA device	
ATAIOWR	O	Write	ATA device	
ATADREQ	I	DMA request	ATA device	
ATADACK	O	DMA acknowledge	ATA device	
ATAIORDY	I	I/O ready	ATA device	
ATAOE	O	Output enable	Bus buffer	Not used
ATADIR	O	Direction	Bus buffer	not used
BYDATA	I	Data input	BY-Chip	
BYDREQ	O	DMA request	BY-Chip	For Stream
BYDACK	1	DMA acknowledge	BY-Chip	For Stream
BYCPUACK	O	DMA acknowledge	BY-Chip	CPUDMA
BYCPUREQ	I	DMA request	BY-Chip	CPUDMA
SDDATA	I/O	Data	SDRAM	
SDADD	O	Address	SDRAM	SDADD13-0
SDCS	O	Chip select	SDRAM	
SDRAS	O	Row address strobe	SDRAM	
SDCAS	O	Column address strobe	SDRAM	
SDWR	O	Write	SDRAM	
CLK54M	I	Clock input	Oscillation circuit	54MHz
CLK54MO	O	Clock output	SDRAM	54MHz
SDCKE	O	Clock enable	SDPAM	
DQML	O	Input mask / Output enable	SDRAM	

■ PD6342A (MAIN ASSY : IC4006)

- Video Pre / Post LSI IC

- **Block Diagram**



● Pin Function (1/7)

No.	Pin Name	I/O	Pin Function
1	SDDATA22	I/O	SDRAM DATA IN/OUT
2	SDDATA21		
3	SDDATA20		
4	SDDATA19		
5	VSS	–	GND
6	VDDI	–	Internal VDD: 2.5V
7	SDDATA18	I/O	SDRAM DATA IN/OUT
8	SDDATA17		
9	SDDATA16		
10	OVSSX0	–	Append GND
11	OVDD3X0	–	Append interface VDD: 3.3V
12	SDTEST7	O	SDRAM I/F TEST output
13	SDTEST6		
14	SDTEST5		
15	SDTEST4		
16	SDTEST3		
17	SDTEST2		
18	VSS	–	GND
19	VDDI	–	Internal VDD: 2.5V
20	SDTEST1	O	SDRAM I/F TEST output
21	SDTEST0		
22	O-PDOUTNE7	O	VIDEO DATA output for NTSC (PAL) ENCODER CCIR656 (8bit, 27MHz) output
23	O-PDOUTNE6		
24	O-PDOUTNE5		
25	VDDE	–	Interface VDD: 3.3V
26	OVSSX1	–	Append GND
27	O-PDOUTNE4	O	VIDEO DATA output for NTSC (PAL) ENCODER CCIR656 (8bit, 27MHz) output
28	O-PDOUTNE3		
29	O-PDOUTNE2		
30	O-PDOUTNE1		
31	O-PDOUTNE0		
32	VSS	–	GND
33	OVDD3X1	O	Append interface VDD: 3.3V
34	O-H-NE	O	HSYNC output for NTSC (PAL) ENCODER
35	O-V-NE	O	VSYSN output for NTSC (PAL) ENCODER
36	O-F-NE	O	FIELD output for NTSC (PAL) ENCODER
37	I-LACT	I	Active line Flag input from VIDEO DECODER. 15Hz input from the DV.
38	I-NONSTDIN	I	Non standard signal Flag input from VIDEO DECODER
39	OVSSX2	–	Append GND
40	VDDE	–	Interface VDD: 3.3V

● Pin Function (2/7)

No.	Pin Name	I/O	Pin Function
41	I-H-ND	I	Connect to GND
42	I-V-ND	I	
43	I-F-ND	I	
44	I-PDINND7	I	Input the decode output of NTSC or PAL VIDEO DECODER CCIR656 (8bit, 27MHz) input
45	I-PDINND6		
46	VSS	–	GND
47	VDDI	–	Internal VDD: 2.5V
48	VCLK	I	27MHz CLK input
49	I-PDINND5	I	Input the decode output of NTSC or PAL VIDEO DECODER CCIR656 (8bit, 27MHz) input
50	I-PDINND4		
51	I-PDINND3		
52	I-PDINND2		
53	I-PDINND1		
54	I-PDINND0		
55	I-PDINDV7	I	Input the decode output of DV I/F DECODER CCIR656 (8bit, 27MHz) input
56	I-PDINDV6		
57	I-PDINDV5		
58	I-PDINDV4		
59	VSS	–	GND
60	VDDI	–	Internal VDD: 2.5V
61	I-PDINDV3	I	Input the decode output of DV I/F DECODER CCIR656 (8bit, 27MHz) input
62	I-PDINDV2		
63	I-PDINDV1		
64	I-PDINDV0		
65	I-CPUADDRESS8	I	CPU ADDRESS input * 16bit
66	I-CPUADDRESS7		
67	I-CPUADDRESS6		
68	I-CPUADDRESS5		
69	I-CPUADDRESS4		
70	I-CPUADDRESS3		
71	XRST	I	Hardware reset input
72	VSS	–	GND
73	I-XACK	I	Acknowledge input at DMA transmission
74	VDDI	–	Internal VDD: 2.5V
75	I-CPUADDRESS2	I	CPU ADDRESS input * 16bit
76	I-CPUADDRESS1		
77	I-CPUADDRESS0		
78	I-XWR	I	Write input from the CPU
79	VDDI	–	Internal VDD: 2.5V
80	OVSSX3	–	Append GND

● Pin Function (3/7)

No.	Pin Name	I/O	Pin Function
81	I-XCS	I	Chip select input from the CPU
82	I-XRD	I	Read input from the CPU
83	CPUDATA15	I/O	CPU DATABUS input/output
84	VSS	–	GND
85	VDDE	–	Interface VDD: 3.3V
86	CPUDATA14	I/O	CPU DATABUS input/output
87	CPUDATA13		
88	CPUDATA12		
89	CPUDATA11		
90	OVSSX4	–	Append GND
91	OVDD3X2	–	Append interface VDD: 3.3V
92	CPUDATA10	I/O	CPU DATABUS input/output
93	CPUDATA9		
94	CPUDATA8		
95	CPUDATA7		
96	VSS	–	GND
97	VDDE	–	Interface VDD: 3.3V
98	CPUDATA6	I/O	CPU DATABUS input/output
99	CPUDATA5		
100	CPUDATA4		
101	CPUDATA3		
102	OVSSX5	–	Append GND
103	OVDD3X3	–	Append interface VDD: 3.3V
104	CPUDATA2	I/O	CPU DATABUS input/output
105	CPUDATA1		
106	CPUDATA0		
107	O-XREQ	O	Request output at DMA transmission
108	VSS	–	GND
109	VDDE	–	Interface VDD: 3.3V
110	O-XIXT1	O	Interrupt output 1 to the CPU
111	O-XIXT2		Interrupt output 2 to the CPU
112	O-F-ME	O	FIELD output for MPEG ENCODER
113	O-V-ME	O	VSYNC output for MPEG ENCODER
114	VDDI	–	Internal VDD: 2.5V
115	OVSSX6	–	Append GND
116	O-H-ME	O	HSYNC output for MPEG ENCODER
117	O-PDOUTME7	O	VIDEO DATA output for MPEG ENCODER CCIR656 (8bit, 27MHz) output
118	O-PDOUTME6		
119	VSS	–	GND
120	O-PDOUTME5	O	VIDEO DATA output for MPEG ENCODER CCIR656 (8bit, 27MHz) output

● Pin Function (4/7)

No.	Pin Name	I/O	Pin Function
121	VDDI	–	Internal VDD: 2.5V
122	O-PDOUTME4	O	VIDEO DATA output for MPEG ENCODER CCIR656 (8bit, 27MHz) output
123	O-PDOUTME3		
124	O-PDOUTME2		
125	O-PDOUTME1		
126	O-PDOUTME0		
127	OVSSX7	–	Append GND
128	OVDD3X4	–	Append interface VDD: 3.3V
129	PLL-L	O	PLL TEST output: OPEN
130	PLL-FB	O	
131	PCO	O	Phase comparison output of TBC
132	TESTOUT7	O	TEST output of video system
133	VSS	–	GND
134	VDDI	–	Internal VDD: 2.5V
135	TESTOUT6	O	TEST output of video system
136	TESTOUT5		
137	TESTOUT4		
138	TESTOUT3		
139	TESTOUT2		
140	OVSS3X8	–	Append GND
141	OVDD3X5	–	Append interface VDD: 3.3V
142	TESTOUT1	O	TEST output of video system
143	TESTOUT0	O	TEST output of video system Output 15Hz /12.5Hz that performed VCLK dividing with TESTMODE=0h.
144	TESTMD3	I	TEST output selection of video system (Normally, use for GND.)
145	TESTMD2		
146	VSS	–	GND
147	VDDI	–	Internal VDD: 2.5V
148	TESTMD1	I	TEST output selection of video system (Normally, use for GND.)
149	TESTMD0		
150	I-H-AV	I	Connect to GND
151	I-V-AV	I	
152	I-F-AV	I	
153	VDDE	–	Interface VDD: 3.3V
154	OVSS3X9	–	Append GND
155	MCLK	I	MCLK input Perform data capture and 656 data output of the DVD decoder with this clock.
156	I-PDINAV7	I	Input the video decode output of DVD (AV) DECODER CCIR656 (8bit, 27MHz) input
157	I-PDINAV6		
158	I-PDINAV5		
159	I-PDINAV4		
160	VSS	–	GND

● Pin Function (5/7)

No.	Pin Name	I/O	Pin Function
161	OVDD3X6	–	Append interface VDD: 3.3V
162	I-PDINAV3	I	Input the video decode output of DVD (AV) DECODER CCIR656 (8bit, 27MHz) input
163	I-PDINAV2		
164	I-PDINAV1		
165	I-PDINAV0		
166	PLL-S	I	PLL RESET input Input a RESET signal.
167	OVSS3X10	–	Append GND
168	VDDE	–	Interface VDD: 3.3V
169	XTCK	I	Internal SCAN and Memory SCAN (JTAG) (Normally, use for VDD.)
170	N.C.	–	Not used
171	VPD	I	Electrostatic discharge prevention terminal Connect to GND.
172	N.C.	–	Not used
173	SDCLKIN	I	81MHz input for SDRAM I/F Input a pin 223 output.
174	VSS	–	GND
175	VDDI	–	Internal VDD: 2.5V
176	TRST	I	Boundary SCAN (JTAG) If these pins are not used, use for VDD or open.
177	TDI	I	
178	TMS	I	
179	TCK	I	
180	OVSS3X11	–	Append GND
181	OVDD3X7	–	Append interface VDD: 3.3V
182	TDO	O	Boundary SCAN (JTAG) If these pins are not used, use for VDD or open.
183	SDDATA15	I/O	SDRAM DATA IN/OUT
184	SDDATA14		
185	SDDATA13		
186	SDDATA12		
187	VSS	–	GND
188	VDDI	–	Internal VDD: 2.5V
189	SDDATA11	I/O	SDRAM DATA IN/OUT
190	SDDATA10		
191	OVSSX12	–	Append GND
192	OVDD3X8	–	Append interface VDD: 3.3V
193	SDDATA9	I/O	SDRAM DATA IN/OUT
194	SDDATA8		
195	SDDATA7		
196	SDDATA6		
197	SDDATA5		
198	SDDATA4		
199	SDDATA3		
200	VSS	–	GND

● Pin Function (6/7)

No.	Pin Name	I/O	Pin Function
201	OVDD3X9	–	Append interface VDD: 3.3V
202	VDDI	–	Internal VDD: 2.5V
203	SDDATA2	I/O	SDRAM DATA IN/OUT
204	SDDATA1		
205	SDDATA0		
206	O-DQM3	O	SDRAM Input Mask/Output Enable 3 output
207	VDDI	–	Internal VDD: 2.5V
208	OVSS13	O	Append GND
209	O-DQM2	O	SDRAM Input Mask/Output Enable 2 output
210	O-DQM1		SDRAM Input Mask/Output Enable 1 output
211	O-DQM0		SDRAM Input Mask/Output Enable 0 output
212	VSS	–	GND
213	VDDE	–	Interface VDD: 3.3V
214	O-BA1	O	SDRAM Bank Select 1 output
215	O-BA0		SDRAM Bank Select 0 output
216	O-XCS-DRAM	O	SDRAM Chip Select
217	O-CKE	O	SDRAM Clock Enable output
218	OVSSX14	–	Append GND
219	OVDD3X10	–	Append interface VDD: 3.3V
220	O-XWE	O	SDRAM Write Enable output
221	O-XRAS	O	SDRAM Row Address Strobe output
222	O-XCAS	O	SDRAM Column Address Strobe output
223	SDCLK	O	81MHz PLL output for SDRAM Input to CLK pin of SDRAM and pin 173 of this LSI.
224	VSS	–	GND
225	VDDE	–	Interface VDD: 3.3V
226	O-SDADDRESS10	O	SDRAM ADDRESS output
227	O-SDADDRESS9		
228	O-SDADDRESS8		
229	O-SDADDRESS7		
230	OVDD3X11	–	Append interface VDD: 3.3V
231	OVSS3X15	–	Append GND
232	O-SDADDRESS6	O	SDRAM ADDRESS output
233	O-SDADDRESS5		
234	O-SDADDRESS4		
235	O-SDADDRESS3		
236	VSS	–	GND
237	VDDE	–	Interface VDD: 3.3V
238	O-SDADDRESS2	O	SDRAM ADDRESS output
239	O-SDADDRESS1		
240	O-SDADDRESS0		

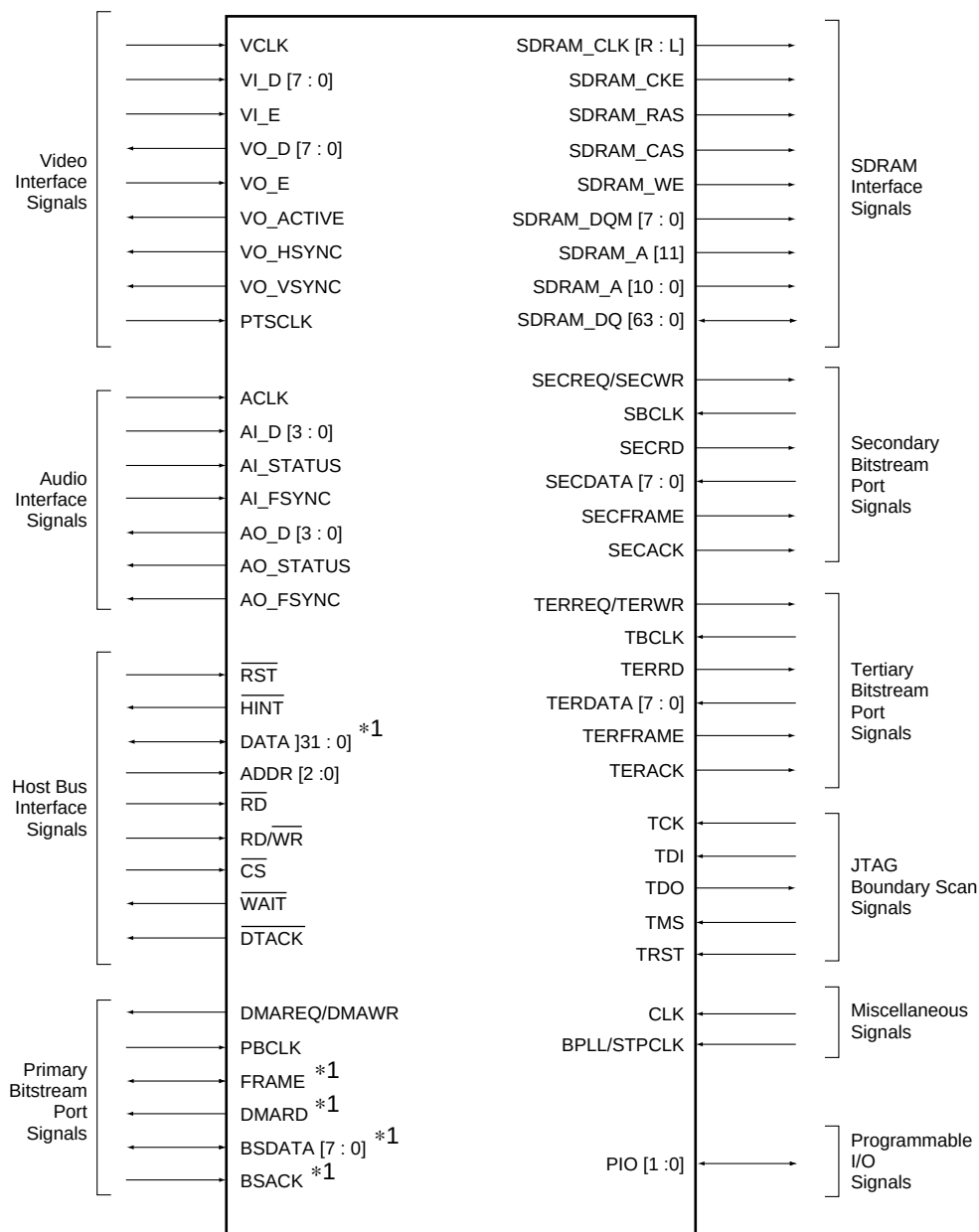
● Pin Function (7/7)

No.	Pin Name	I/O	Pin Function
241	SDDATA31	I/O	SDRAM DATA IN/OUT
242	VDDI	–	Internal VDD: 2.5V
243	OVSSX16	–	Append GND
244	SDDATA30	I/O	SDRAM DATA IN/OUT
245	SDDATA29		
246	SDDATA28		
247	VSS	–	GND
248	OVDD3X12	–	Append interface VDD: 3.3V
249	VDDI	–	Internal VDD: 2.5V
250	SDDATA27	I/O	SDRAM DATA IN/OUT
251	SDDATA26		
252	SDDATA25		
253	SDDATA24		
254	SDDATA23		
255	OVSSX17	–	Append GND
256	OVDDX13	–	Append interface VDD: 3.3V

■ DVXCEL-BA1 (MAIN ASSY : IC5005)

• MPEG2 Video Codec

• Block Diagram



*1 :

Note that BSDATA [7 : 0] share pins with DATA [28 : 21], BSACK shares a pin with DATA [31], FRAME shares a pin with DATA [30], and DMARD shares a pin with DATA [29].

● Pin Function

Mark	Pin Name	I/O	Pin Function
Host Bus I/F			
XRST	Y19	I	Chip Reset
XHINT	V17	O	Host Interrupt Request
DATA [31 : 16]	V5, W4, Y3, V6, W5, Y5, V7, W6, Y6, W7, V8, Y7, W8, V9, Y8, W9	I/O TS	32-bit host interface data bus upper 16 bits. Upper 11 bits shared with BSACK (Data[31]), FRAME (Data[30]), DMARD (Data[29]) and BSDData[7:0](Data[28:21]) pins.
DATA [15 : 0]	Y9, V10, W10, Y10, Y11, W11, Y12, W12, V11, Y13, V12, W13, Y14, W14, Y15, V14	I/O TS	Lower 16 bits host interface data bus
ADDR [2 : 0]	V16, Y18, W15	I	Host Address bus (16-bit word address)
XRD	Y16	I	Host I-mode Write strobe/M-mode direction signal
XCS	V15	I	Host Chip Select
XWAIT	W18	O	Host Ready
XDTACK	W17	O	Host Data Transfer Acknowledge
Primary Bitstream I/F			
DMAREQ/DMAWR	Y17	O	Host DMA or Primary Bitstream port transfer request or write transfer request
PBCLK	Y4	I	Separate Primary Bitstream port clock, 0 - 27 MHz
FRAME	W4	I/O TS	Separate Primary Bitstream start of packet
DMARD	Y3	O	Separate Primary Bitstream port, outgoing transfer
BSDATA [7 : 0]	V6, W5, Y5, V7, W6, Y6, W7, V8	I/O TS	Separate bitstream port data
BSACK	V5	I	Separate bitstream transfer grant
Secondary Bitstream I/F			
SBCLK	Y1	I	Secondary bitstream port clock, 0 - 27 MHz
SECRD	U1	O	Secondary bitstream port, outgoing transfers
SECDATA [7 : 0]	T3, U2, W2, V3, U3, V4, W3, Y2	I/O TS	Secondary bitstream port data
SECFRAME	V2	I/O TS	Secondary bitstream start of packet frame
SECACK	W1	I	Secondary bitstream transfer grant
SECREQ/SECWR	V1	O	Secondary bitstream port transfer or write transfer request
Tertiary Bitstream I/F			
TBCLK	L1	I	Tertiary bitstream port clock, 0 - 27 MHz
TERRD	G2	O	Tertiary bitstream port, outgoing transfers
TERDDATA [7 : 0]	J2, J1, K2, K1, L2, K3, L3, M2	I/O TS	Tertiary bitstream port data
TERFRAME	H1	I/O TS	Tertiary bitstream start of packet frame
TERRACK	H2	I	Tertiary bitstream transfer grant
TERREQ/TERWR	G1	O	Tertiary bitstream port transfer or write transfer request

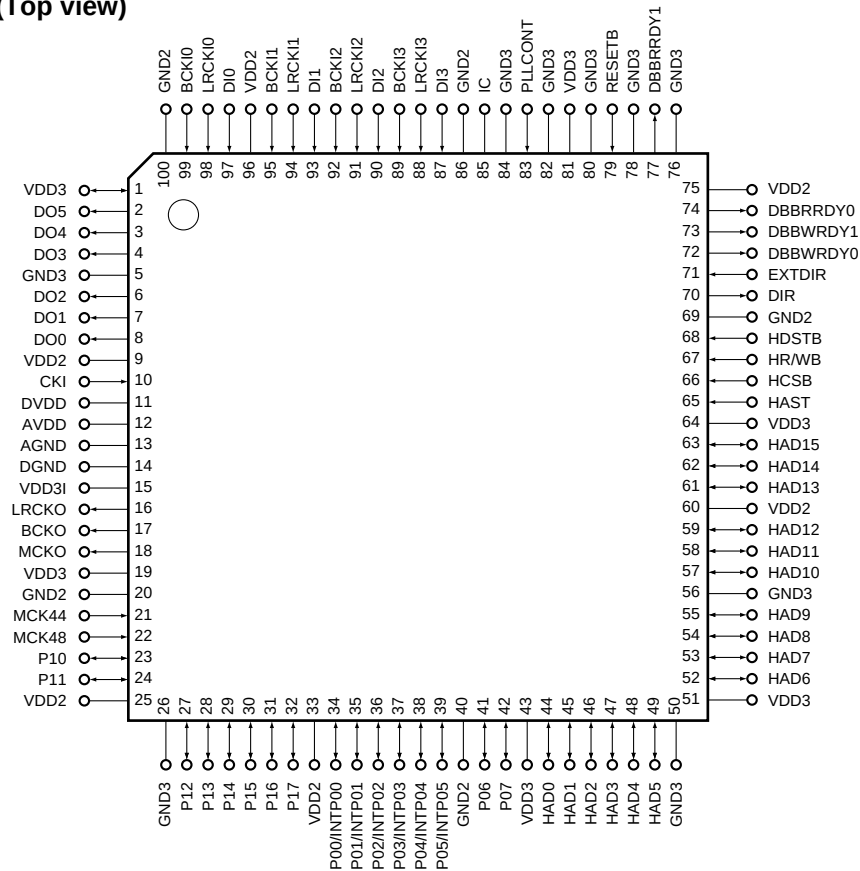
Mark	Pin Name	I/O	Pin Function
Video I/F			
PTSCCLK	M1	I	Video PTS Clock. This required clock is timing reference for the internal presentation timestamp (PTS) counter. The external PTS clock frequency is either 27 MHz or 90 kHz. The internal frequency is 90 kHz. Microcode autodetects the PTS clock frequency and adjusts its internal divider appropriately. PTSCCLK is asynchronous to all other processor clocks. C-Cube recommends that your board include parallel AC termination or DC termination to terminate this clock's source driver.
VCLK	T20	I	Video Clock. VCLK is the video input/output sampling clock. Input data is sampled and output data is driven on the rising edge of VCLK. Valid VCLK frequencies are 27 MHz and 54 MHz. VCLK is asynchronous to all other processor clocks.
VI_D [9 : 0]	M20, M19, M18, N20, N19, P20, N18, P19, R20, R18	I	Video input Data. These pins capture the interleaved luma and chroma samples (4 : 2 : 0 format). Micro-code determines whether the data order is (Cb, Y, Cr, Y) or (Y, Cb, Y, Cr). The DVxcel processor decodes the SAV codes in the incoming video data to determine whether the video is active and whether the field is odd or even. For 8-bit input, drive data onto pins VI_D [9 : 2] and ground pins VI_D [1 : 0].
VI_E	P18	I	Video Input Enable. When VI_E is asserted, the DVxcel processor samples input pels on the VI_D bus and increments the horizontal position counter. This signal allows external downsampling hardware to throttle video capture without generating a nonstandard video clock.
VO_ACTIVE	R19	O TS VC	Video Output Active. The DVxcel processor asserts VO_ACTIVE when an active (nonblanked) pel is present on the VO_D bus.
VO_D [7 : 0]	U19, V20, T19, V19, W20, W19, U18, Y20	O TS VC	Video Output Data. The DVxcel processor outputs interleaved luma and chroma samples (4 : 2 : 0 format) on these pins. Microcode determines whether the data order is either (Cb, Y, Cr, Y) or (Y, Cb, Y, Cr). The DVxcel processor inserts an SAV code with the appropriate V and F bits into the output stream starting four clocks before VO_ACTIVE is asserted. The V bit in the SAV code is set to one during vertical blanking. The F bit is set to one when the current field is even. The DVxcel processor inserts an EAV code into the output stream starting on the clock that VO_ACTIVE is deasserted.
VO_E	V18	I	Video Output Enable. When VO_E is asserted, the output value and horizontal position are held to the same value as in the previous clock, if the video output was not blanked during that clock. VO_E allows external hardware to throttle video output without generating a nonstandard video clock. VO_E is ignored with echo active. VO_E can be used with genlock or video capture active as long as the time to transfer the last active pel is less than the total input frame time.
VO_HSYNC	U20	O TS VC	Video Horizontal Synchronization. The DVxcel processor asserts VO_HSYNC at the first pel in each line for the duration specified by the microcode. Note that the polarity of this output is programmable via the OSPOL bit in the Video Control Register.
VO_VSYNC	T18	O TS VC	Video Vertical Synchronization. The DVxcel processor asserts VO_VSYNC at the beginning of an odd field and holds it asserted for the number of lines specified by the microcode. For interlaced transfer, the processor asserts VO_VSYNC starting in the middle of the last scan line of an odd field. VO_VSYNC is then deasserted in the middle of the scan line after the number of lines specified by the microcode (next even field). Note that the polarity of this output is programmable via the OSPOL bit in the Video Control Register.

Mark	Pin Name	I/O	Pin Function
SDRAM I/F			
XSDRAM_CAS	B12	O	SDRAM Column Address Strobe.
XSDRAM_RAS	C12	O	SDRAM Row Address Strobe.
SDRAM_A [11]	B8	O	SDRAM Bank Address This output determines which SDRAM bank is selected.
SDRAM_A [10 : 0]	A8, C9, B9, A9, C10, B10, A10, A11, B11, C11, A12	O	SDRAM Address
SDRAM_CLK [R : L]	A13, B7	O	SDRAM Clock. These outputs are buffered versions of the internal processor clock. SDRAM_CLKR and SDRAM_CLKL are identical. Two outputs are provided to reduce the output loading and simplify PCB layout.
SDRAM_CKE	B13	O	SDRAM Clock Enable.
XSDRAM_WE	C13	O	SDRAM Write Enable.
SDRAM_DQM [7 : 0]	A6, C7, A7, C8, A14, B14, A15, C14	O	SDRAM Data Mask (Byte Enables). These bits connect directly to the appropriate UDQM/LDQM inputs. SDRAM_DQM0 controls the most-significant byte; SDRAM_DQM7 controls the least-significant byte. They are used for partial stores and termination of burst write transfers.
SDRAM_DQ [63 : 0]	F20, G20, F19, E20, F18, E19, D20, D19, G17, C20, B20, E18, C19, D18, A20, E17, C18, D17, A19, B19, C17, D16, A18, B18, B17, C16, D15, A17, B16, C15, A16, B15, B6, C6, A5, B5, A4, C5, D6, A3, B4, B3, A2, C4, D5, E4, C3, B2, A1, F4, B1, D3, C2, E3, G4, D2, C1, D1, F3, E2, E1, F2, G3, F1	I/O TS	SDRAM Data.
Audio I/F			
ACLK	N1	I	Audio Clock. ACLK is the serial clock used for audio input and output. Input data is sampled on and output data is driven on the active edge of ACLK. Microcode determines whether the active edge is the rising or the falling edge. ACLK is asynchronous to all other DVxcel processor clocks. Its maximum frequency is 9.09 MHz. The frequency of ACLK and the number of clocks per sample depend on the audio frame format selected.
AI_D [3 : 0]	P1, M3, N2, N3	I	Audio Input Data. Up to eight channels of serial audio data are clocked into the AI_D [3 : 0] pins. With two samples per frame, channels 2n and (2n + 1) use pin AI_Dn. With one sample per frame, channel n uses pin AI_Dn. Microcode determines the number of samples per frame. The processor samples AI_D [3:0] on the active edge of ACLK.
AI_FSYNC	P2	I	Audio Frame Sync In. Asserting AI_FSYNC indicates the start or end of the next input sample or frame as specified by the selected audio frame format (Section 9.2). The processor samples AI_FSYNC on the active edge of ACLK.
AI_STATUS	P3	I	Audio Input Status. Audio status information (32 bits for each sample frame) is clocked in on the active edge of ACLK.
AO_D [3 : 0]	R3, T2, R1, R2	O	Audio Output Data. The DVxcel processor clocks up to eight channels of serial audio data from the four AO_D outputs. With two samples per frame, channels 2n and (2n + 1) use pin AO_Dn. With one sample per frame, channel n uses pin AO_Dn. Microcode determines the number of samples per fram. AO_D [3 : 0] are driven on the active edge of ACLK.
AO_FSYNC	T1	O	Audio Frame Sync Out. The DVxcel processor asserts AO_FSYNC as an indicator of the start or end of the next output sample or frame as specified by the selected audio frame format.
AO_STATUS	R4	O	Audio Output Status. Audio status information (32 bits for each sample frame) is clocked out of the DVxcel processor on the active edge of ACLK.

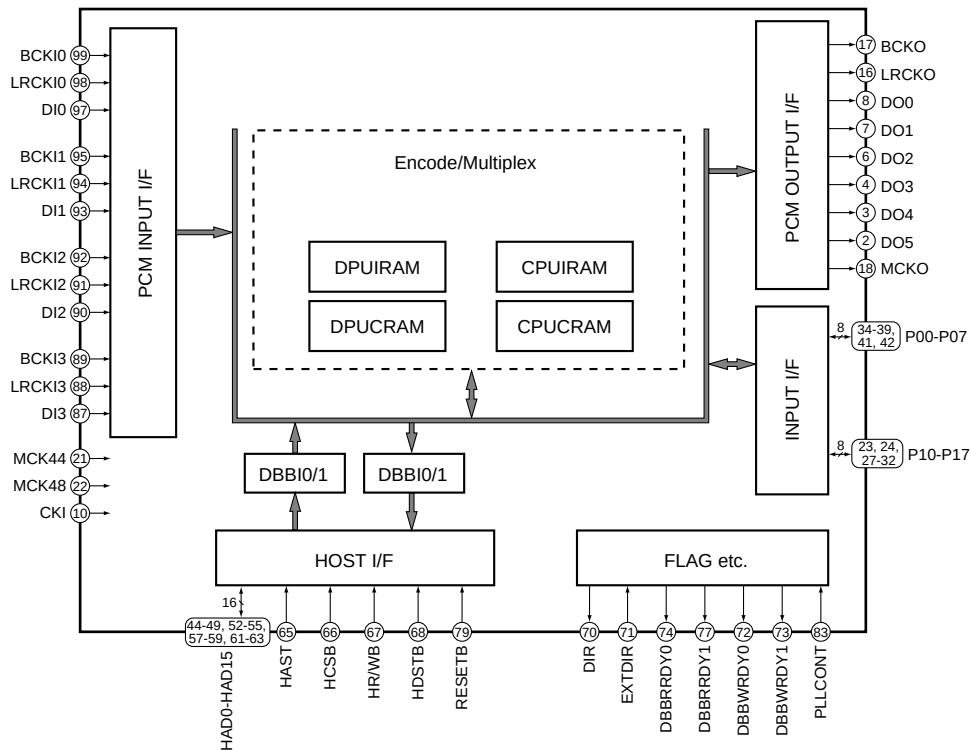
Mark	Pin Name	I/O	Pin Function
JTAG Boundary Scan I/F			
TCK	K20	I	JTAG Test Clock. This input clocks state information, boundary scan instructions, and test data into and out of the DVxcel processor during Test Access Port (TAP) operation.
TDI	K18	I	JTAG Test Data In. Test data and test instructions are shifted serially into this input during TAP operation.
TDO	L19	O TS	JTAG Test Data Out. Test data and test instructions are shifted serially out of this output during TAP operation.
TMS	L18	I PUP	JTAG Test Mode Select. This input controls the state of the DVxcel processor's TAP controller.
XTRST	K19	I PUP	JTAG Test Reset. Asynchronously asserting this input causes the DVxcel processor to initialize the TAP controller. If the JTAG port is not used, tie this input LOW. Otherwise, pull it down with a 470 Ω resistor.
Miscellaneous			
BPLL/STPCLK	H20	I	Bypass PLL/Stop Clock. A LOW on this input selects PLL/2 output to drive the internal processor clock, and a HIGH selects the CLK input pin to drive the internal processor clock. The select value is latched on the deassertion of XTRST and is used until the DVxcel processor is externally reset again. For normal system operation, tie this input LOW to select the PLL/2 output.
CLK	J20	I	Internal Clock Reference. The internal processor clock uses this input as the timing reference. CLK is normally 27.5 MHz. It is internally multiplied by 8 and divided by 2 to yield the 110 MHz internal clock C-Cube recommends that your board include parallel AC termination or DC termination to terminate this clock's source driver.
Programmed I/O			
PIO [1 : 0]	J3, H3	I/O	Programmed I/O. These pins are individually programmed as inputs or outputs through the Programmed I/O Register. 4.7 k Ω pullup resistors should be connected to +3.3V.
Power, Ground and No Connect			
C_V	H18	O	Clock VCO Control Voltage, used for testing purposes. Leave open (NC).
VDD	D7-D14, E9-E12, J5, J16, K5, K16, L5, L16, M5, M16, T9-T12, U7-U14	–	3.3V Digital Power. These pins are the primary power supply for the input and output voltages of non-host interface pads.
VDD_A	G18	–	3.3V Analog Power for the Internal Clock PLL. This pin provides the analog power for the DVxcel processor's internal clock phase locked loop.
VDDQ	D4, F17, H4, H17, J4, J17, K4, L17, M4, N4, N17, P4, P17, T17	–	1.9V Digital Power. These pins supply power to the core. They have been separated from the standard power supply pins so that you can add extra decoupling, if needed.
VDD_P	G19	–	3.3V Digital Power for the Internal Clock PLL. This pin provides digital power to the DVxcel processor's internal clock phase locked loop. Connect it to the system power plane.
GND	H8-H13, J8-J13, K8-K13, L8-L13, M8-M13, N8-N13	–	Digital Ground. These pins are the primary ground pins for the logic on the DVxcel processor.
GND_A	J18	–	Analog Ground for the Internal Clock PLL. This pin provides the analog ground for the DVxcel processor's internal clock phase locked loop.
GND_P	H19	–	Digital Ground for the Internal Clock PLL. This pin provides ground to the DVxcel processor's internal clock phase locked loop. Connect it to the system ground plane.
NC	J19, K17, L4, L20, M17, R17, T4, U4-U6, U15-U17, V13	–	No Connect.

■ UPD61003 (MAIN ASSY : IC6002)

- DDCE
- Pin Assignment (Top view)



• Block Diagram



● Pin Function

No.	Pin Name	I/O	Pin Function
1	VDD3	I/O	+3.3V power supply
2	DO5	O	PCM output data 5
3	DO4		PCM output data 4
4	DO3		PCM output data 3
5	GND3	–	Ground (3.3V)
6	DO2	O	PCM output data 2
7	DO1		PCM output data 1
8	DO0		PCM output data 0
9	VDD2	–	+2.5V power supply
10	CKI	I	System clock input
11	DVDD	–	+2.5V power supply (for divider of internal PLL circuit)
12	AVDD	–	+2.5V power supply (for analog circuit of internal PLL circuit)
13	AGND	–	Ground (for analog circuit of internal PLL circuit)
14	DGND	–	Ground (for digital circuit of internal PLL circuit)
15	VDD3I	–	+3.3V power supply
16	LRCKO	O	Common LRCK for PCM output 0 through 5
17	BCKO	O	Common bit clock for PCM output 0 through 5
18	MCKO	O	Audio master clock output Output 256fs or 384fs in accordance with the setting of the PCM mode register.
19	VDD3	–	+3.3V power supply
20	GND2	–	Ground (2.5V)
21	MCK44	I	Audio master clock input (for 44.1kHz) Input 256fs or 384fs in accordance with the setting of the PCM mode register.
22	MCK48	I	Audio master clock input (for 32kHz, 48kHz) Input 256fs or 384fs in accordance with the setting of the PCM mode register.
23	P10	I/O	General-purpose I/O ports If any of these pins are connected to a high impedance (1M Ω min.), pull it down or up with a resistance of 1k Ω or higher.
24	P11		
25	VDD2	–	+2.5V power supply
26	GND3	–	Ground (3.3V)
27	P12	I/O	General-purpose I/O ports If any of these pins are connected to a high impedance (1M Ω min.), pull it down or up with a resistance of 1k Ω or higher.
28	P13		
29	P14		
30	P15		
31	P16		
32	P17		
33	VDD2	–	+2.5V power supply
34	P00/INTP00	I/O	General-purpose I/O ports If any of these pins are connected to a high impedance (1M Ω min.), pull it down or up with a resistance of 1k Ω or higher.
35	P01/INTP01		
36	P02/INTP02		
37	P03/INTP03		
38	P04/INTP04		
39	P05/INTP05	I	/External maskable interrupt inputs Detected at rising edge.
40	GND2	–	Ground (2.5V)
41	P06	I/O	General-purpose I/O ports If any of these pins are connected to a high impedance (1M Ω min.), pull it down or up with a resistance of 1k Ω or higher.
42	P07		
43	VDD3	–	+3.3V power supply
44	HAD0	I/O	Host address/data bus
45	HAD1		
46	HAD2		
47	HAD3		
48	HAD4		
49	HAD5		
50	GND3	–	Ground (3.3V)

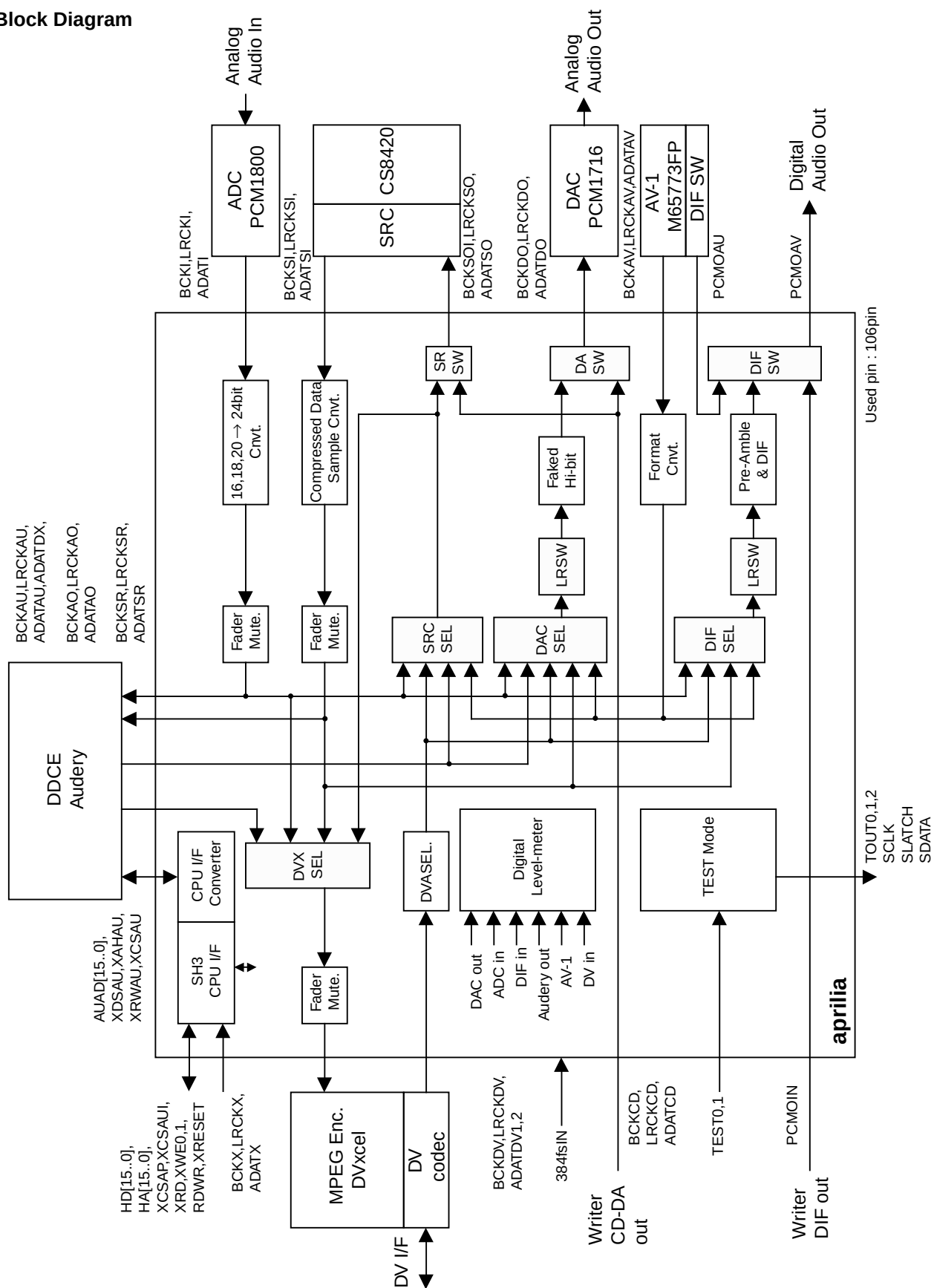
DVR-7000

No.	Pin Name	I/O	Pin Function
51	VDD3	–	+3.3V power supply
52	HAD6	I/O	Host address/data bus
53	HAD7		
54	HAD8		
55	HAD9		
56	GND3	–	Ground (3.3V)
57	HAD10	I/O	Host address/data bus
58	HAD11		
59	HAD12		
60	VDD2	–	+2.5V power supply
61	HAD13	I/O	Host address/data bus
62	HAD14		
63	HAD15		
64	VDD3	–	+3.3V power supply
65	HAST	I	Host address strobe
66	HCSB	I	Chip select
67	HR/WB	I	Host read/write status
68	HDSTB	I	Host data strobe
69	GND2	–	Ground (2.5V)
70	DIR	O	HAD bus drive controll flag output This flag indicates the bus driving direction of HAD15 through HAD0. "H": output, "L": input
71	EXTDIR	I	HAD bus drive control flag This pin controls the bus drive control flag from DIR. Connect this pin to GND.
72	DBBWRDY0	O	DBBI0 write ready flag This flag enables write access to the DBBI0 resistor. Writing is enabled when this flag is high and disabled when it is low.
73	DBBWRDY1		DBBI1 write ready flag This flag enables write access to the DBBI1 resistor. Writing is enabled when this flag is high and disabled when it is low.
74	DBBRRDY0	O	DBBO0 read ready flag This flag enables read access to the DBBO0 resistor. Reading is enabled when this flag is high and disabled when it is low.
75	VDD2	–	+2.5V power supply
76	GND3	–	Ground (3.3V)
77	DBBRRDY1	O	DBBO1 read ready flag This flag enables read access to the DBBO1 resistor. Reading is enabled when this flag is high and disabled when it is low.
78	GND3	–	Ground (3.3V)
79	RESETB	I	System reset
80	GND3	–	Ground (3.3V)
81	VDD3	–	+3.3V power supply
82	GND3	–	Ground (3.3V)
83	PLLCONT	I	PLL operation mode If this pin is connected to GND (PLL mode), the internal operating clock frequency is two times higher than of the clock input to the CKI pin. If it is connected to DVDD3 (direct mode), the internal operating clock frequency is equal to that of the clock input to the CKI pin. Usually, use the PLL mode by connecting this pin to GND.
84	GND3	–	Ground (3.3V)
85	IC	–	Open
86	GND2	–	Ground (2.5V)
87	DI3	I	PCM input data 3
88	LRCKI3	I	LRCK for PCM input 3
89	BCKI3	I	Bit clock for PCM input 3
90	DI2	I	PCM input data 2
91	LRCKI2	I	LRCK for PCM input 2
92	BCKI2	I	Bit clock for PCM input 2
93	DI1	I	PCM input data 1
94	LRCKI1	I	LRCK for PCM input 1
95	BCKI1	I	Bit clock for PCM input 1
96	VDD2	–	+2.5V power supply
97	DI0	I	PCM input data 0
98	LRCKI0	I	LRCK for PCM input 0
99	BCKI0	I	Bit clock for PCM input 0
100	GND2	–	Ground (2.5V)

PE7004A (MAIN ASSY : IC6003)

• Audio I/F IC

• Block Diagram



● Pin Function (1/2)

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function		
1	VDD	–	VDD	49	HA10	I	CPU I/F Address		
2	TMS	–	JTAG	50	HA9				
3	TDO	–		51	HA8				
4	TRST	–		52	GND	–	GND		
5	TEST0	I	TEST	53	VDD	–	VDD		
6	TEST1			54	HA7	I	CPU I/F Address		
7	TOUT0	O		55	HA6				
8	TOUT1			56	HA5				
9	TOUT2			57	HA4				
10	SCLK			58	HA3				
11	SDATA			59	HA2				
12	SLATCH			60	HA1				
13	GND	–	GND	61	HA0				
14	VDD	–	VDD	62	GND	–	GND		
15	PCMOIN	I	ADIF from the drive	63	VDD	–	VDD		
16	LRCKCD		Audio signal LRCK from the drive	64	HD15	I/O	CPU I/F Data		
17	BCKCD		Audio signal BCK from the drive	65	HD14				
18	ADATCD		Audio signal DATA from the drive	66	HD13				
19	LRCKX	O	Audio signal LRCK to the Dvxccl	67	HD12				
20	BCKX		Audio signal BCK to the Dvxccl	68	HD11				
21	ADATX		Audio signal DATA to the Dvxccl	69	HD10				
22	LRCKDV	I	Audio signal LRCK from the Dvxccl	70	HD9				
23	BCKDV		Audio signal BCK from the Dvxccl	71	HD8				
24	ADATDV1		Audio signal DATA from the Dvxccl	72	GND	–	GND		
25	ADATDV2		Audio signal DATA from the Dvxccl	73	VDD	–	VDD		
26	GND	–	GND	74	HD7	I/O	CPU I/F Data		
27	VDD	–	VDD	75	HD6				
28	LRCKAV	I	Audio signal LRCK from the AV1	76	HD5				
29	BCKAV		Audio signal BCK from the AV1	77	HD4				
30	ADATAV		Audio signal DATA from the AV1	78	HD3				
31	PCMOAV	O	ADIF output	79	HD2				
32	XRESET	I	Chip reset	80	HD1				
33	XCSAUI		CS to Audery	81	HD0				
34	XCSAP		Aprilia CS	82	GND	–	GND		
35	RDWR		CPU I/F RDWR	83	VDD	–	VDD		
36	GND	–	GND	84	AUAD15	I/O	Audery Bus		
37	VDD	–	VDD	85	AUAD14				
38	CLK40M	I	CLK for CPU I/F	86	AUAD13				
39	XWRL		CPU I/F WR L byte	87	AUAD12				
40	XWRH		CPU I/F WR H byte	88	AUAD11				
41	XRD		CPU I/F RD	89	AUAD10				
42	GND	–	GND	90	AUAD9				
43	VDD	–	VDD	91	AUAD8				
44	HA15	I	CPU I/F Address	92	GND	–	GND		
45	HA14			93	VDD	–	VDD		
46	HA13			94	AUAD7	I/O	Audery Bus		
47	HA12			95	AUAD6				
48	HA11			96	AUAD5				

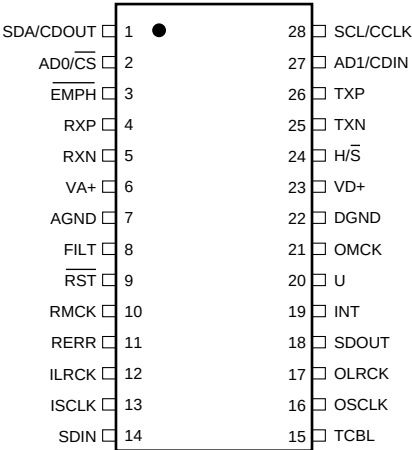
● Pin Function (2/2)

No.	Pin Name	I/O	Pin Function
97	AUAD4	I/O	Audery Bus
98	AUAD3		
99	AUAD2		
100	AUAD1		
101	AUAD0		
102	GND	–	GND
103	VDD	–	VDD
104	XAHAU	O	Address hold signal of Audery
105	XDSAU		Data hold signal of Audery
106	XRWAU		Audery RW
107	XCSAU		Audery CS
108	GND	–	GND
109	VDD	–	VDD
110	LRCKAU	I	Audio signal LRCK from the Audery
111	BCKAU		Audio signal BCK from the Audery
112	ADATAU		Audio signal DATA from the Audery
113	ADATDX		Audio signal DATA from the Audery
114	PCMOAU		ADIF signal from the AV1
115	LRCKSR	O	Audio signal LRCK to the Audery
116	BCKSR		Audio signal BCK to the Audery
117	ADATSR		Audio signal DATA to the Audery
118	LRCKAO		Audio signal LRCK to the Audery
119	BCKAO		Audio signal BCK to the Audery
120	ADATAO		Audio signal DATA to the Audery
121	GND	–	GND
122	VDD	–	VDD
123	CLK36M	I	CLK for Audio system circuit
124	LRCKDO	O	Audio signal LRCK to the DAC
125	BCKDO		Audio signal BCK to the DAC
126	ADATDO		Audio signal DATA to the DAC
127	LRCKI	I	Audio signal LRCK from the ADC
128	BCKI		Audio signal BCK from the ADC
129	ADATI		Audio signal DATA from the ADC
130	GND	–	GND
131	VDD	–	VDD
132	LRCKSI	I	Audio signal LRCK from the SRC
133	BCKSI		Audio signal BCK from the SRC
134	ADATSI		Audio signal DATA from the SRC
135	LRCKSO	O	Audio signal LRCK to the SRC
136	BCKSO		Audio signal BCK to the SRC
137	ADATSO		Audio signal DATA to the SRC
138	GND	–	GND
139	VDD	–	VDD
140	ATPGEN	–	IC TEST
141	SCANEN	–	IC TEST
142	TCK	–	JTAG
143	TDI	–	JTAG
144	GND	–	GND

CS8420-CS (MAIN ASSY : IC6004)

• Sampling Rate Converter

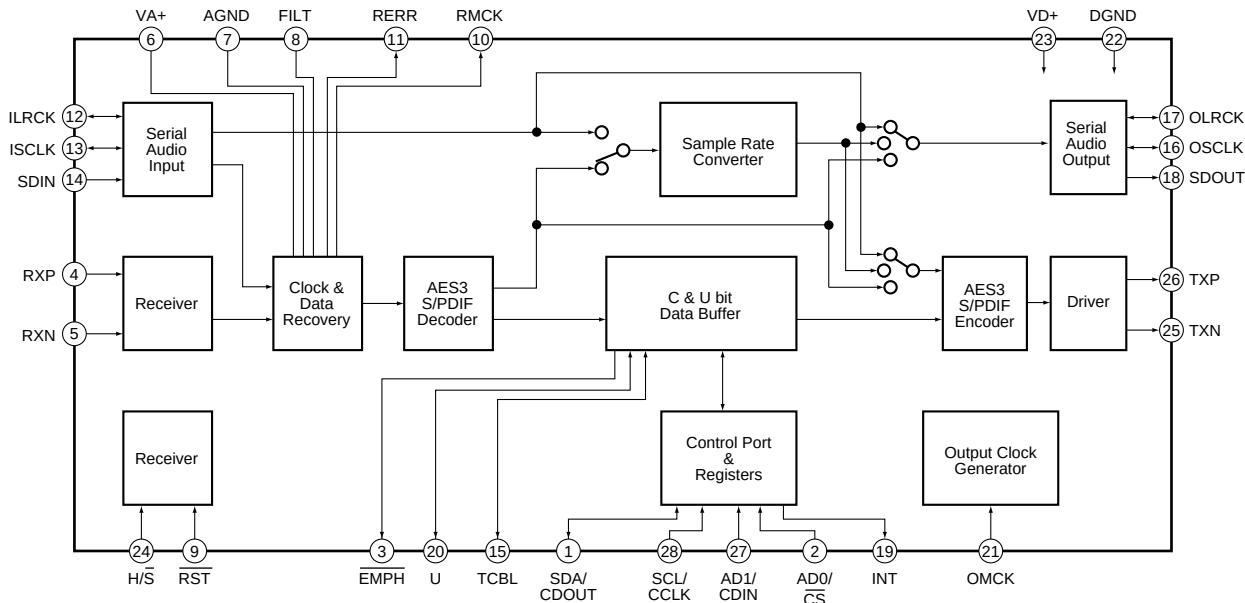
• Pin Assignment (Top view)



• Pin Function

No.	Pin Name	I/O	Pin Function
1	SDA/CDOUT	O	Serial control data I/O (I ² C) / data out (SPI)
2	AD0/CS	I	Address bit 0 (I ² C) / Control port chip select (SPI)
3	EMPH	O	Pre-emphasis indicator output
4	RXP	I	Differential line receiver inputs
5	RXN		
6	VA+	-	Positive analog power (+5V)
7	AGND	-	Analog ground
8	FILT	-	PLL loop filter
9	RST	I	Reset input
10	RMCK	O	Input section recovered master clock output
11	RERR	O	Receiver error indicator
12	ILRCK	I/O	Serial audio input port L/R clock input or output
13	ISCLK	I/O	Serial audio input port bit clock input or output
14	SDIN	I	Serial audio input port data input
15	TCBL	O	Transmit channel status block start
16	OSCLK	I/O	Serial audio output port bit clock input or output
17	OLRCK	I/O	Serial audio output port L/R clock input or output
18	SDOUT	O	Serial audio output port data output
19	INT	O	Interrupt output
20	U	O	User data
21	OMCK	I	Outout section master clock input
22	DGND	-	Digital ground
23	VD+	-	Positive digital power (+5V)
24	H/S	I	Hardware or software control mode select
25	TXN	O	Differential line driver outputs
26	TXP		
27	AD1/CDIN	I	Address bit 1 (I ² C) / Control port chip select (SPI)
28	SCL/CCLK	I	Control port clock

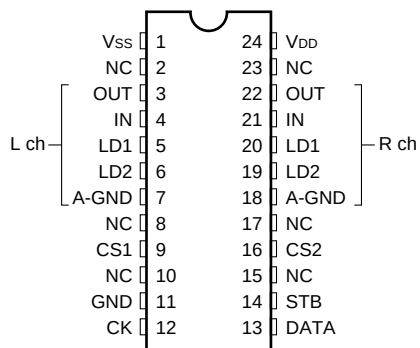
• Block Diagram



■ TC9412AF (MAIN ASSY : IC8002)

- ER-VR IC

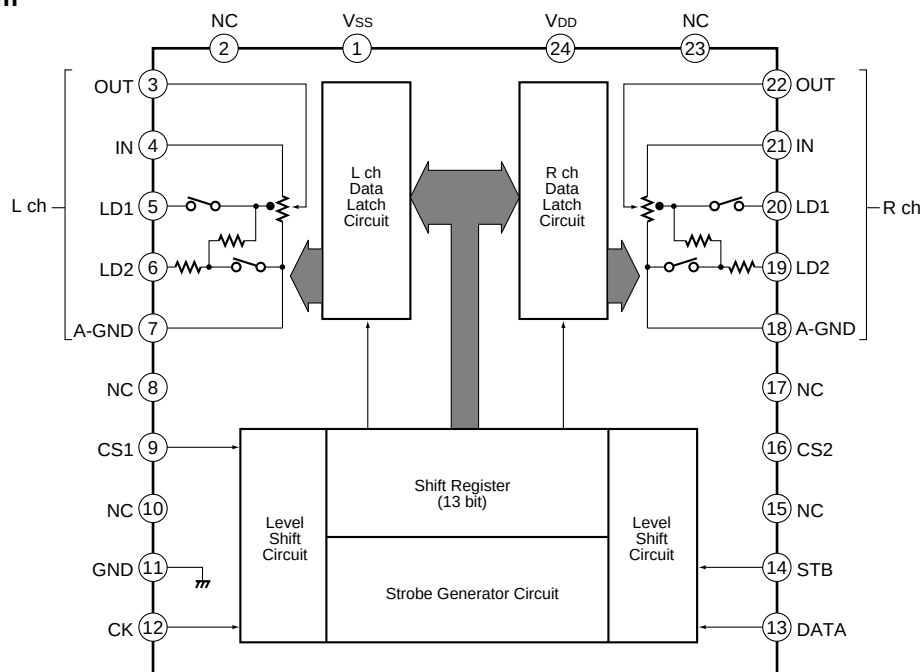
- **Pin Assignment (Top view)**



- **Pin Function**

Pin	Pin Name	Pin Function
1	Vss	Negative power supply pin
2	NC	Non connection pin
3	OUT	L ch Volume output pin
4	IN	L ch Volume input pin
5	LD1	L ch Loudness tap output pin
6	LD2	L ch Loudness tap output pin
7	A-GND	L ch Analog ground pin
8	NC	Non connection
9	CS1	Chip select input pin
10	NC	Non connection
11	GND	Digital ground pin
12	CK	Clock input pin
13	DATA	Data input pin
14	STB	Strobe input pin
15	NC	Non connection
16	CS2	Chip select input pin
17	NC	Non connection
18	A-GND	R ch Analog ground pin
19	LD2	R ch Loudness tap output pin
20	LD1	R ch Loudness tap output pin
21	IN	R ch Volume input pin
22	OUT	R ch Volume output pin
23	NC	Non connection
24	V _{DD}	Positive power supply pin

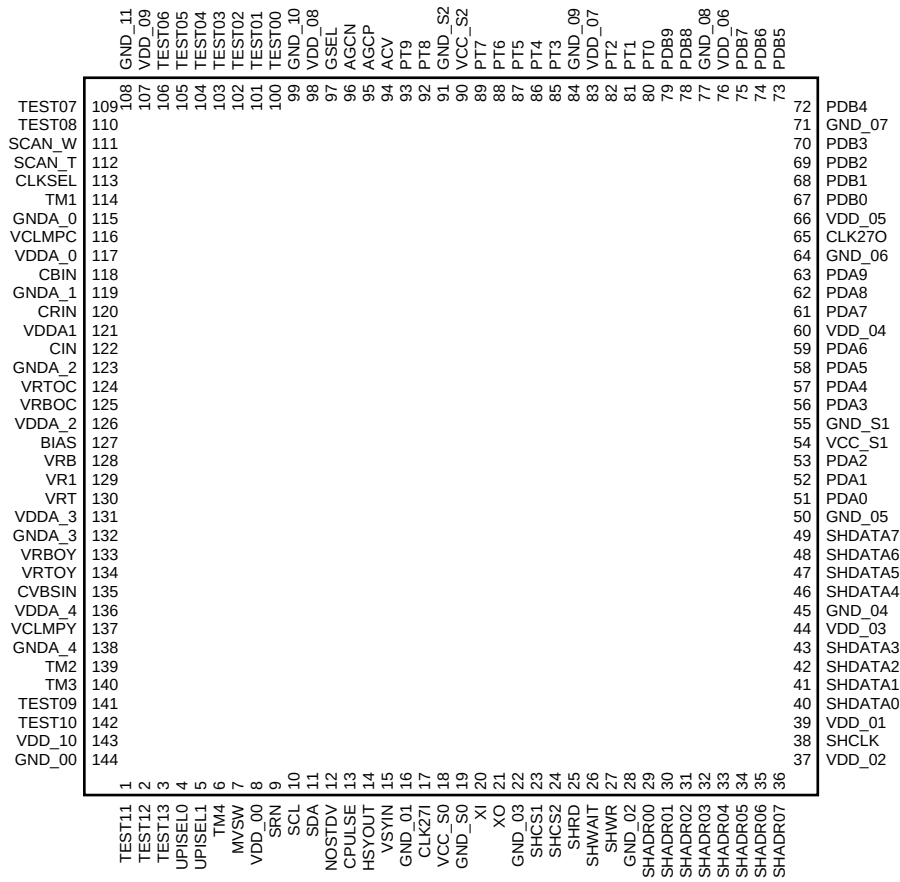
- **Block Diagram**



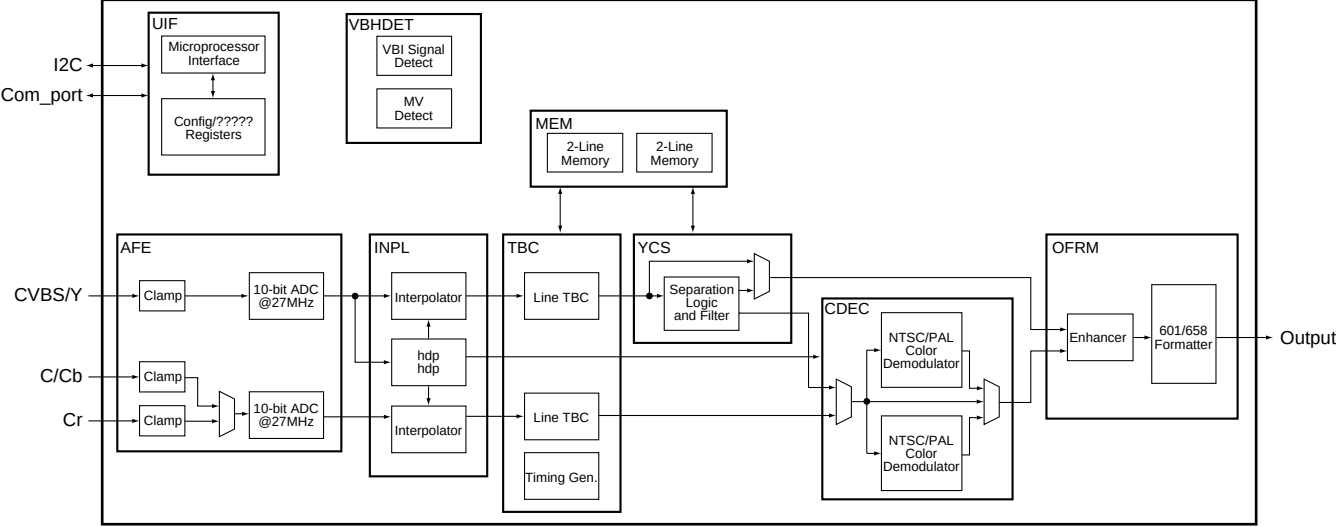
PD0272A (MAIN ASSY : IC8008)

• Video Decoder IC

• Pin Assignment (Top view)



• Block Diagram



● Pin Function

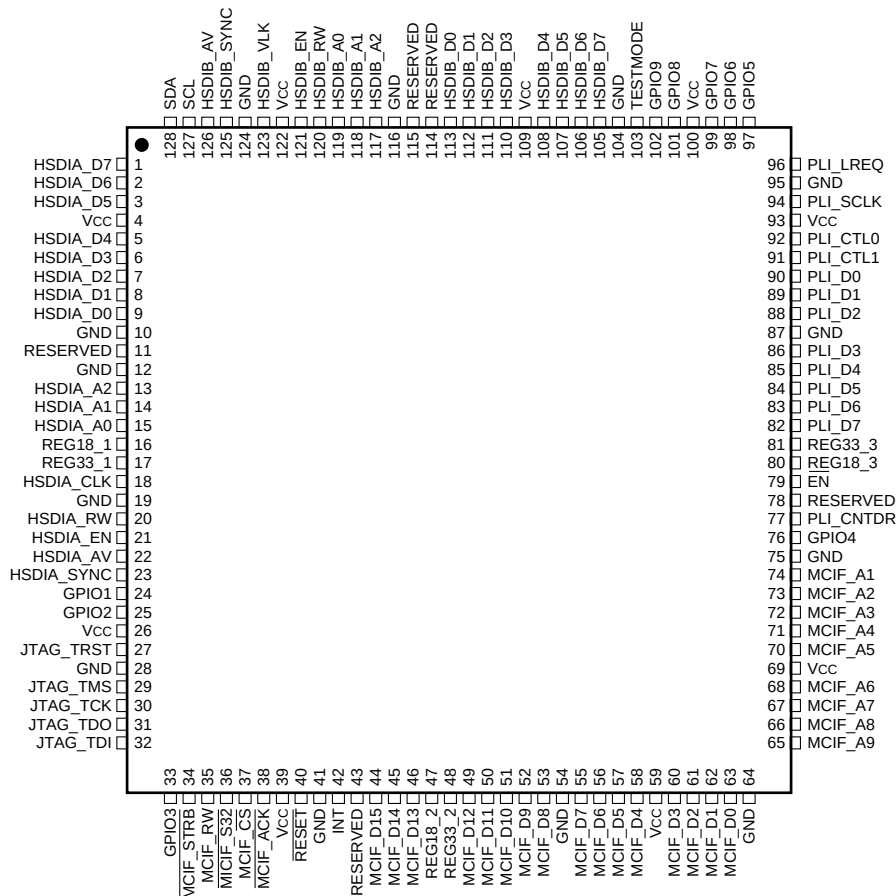
No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
1	TEST11	I/O	Reserved for Test	37	VDD_02	–	[PAD] VDD
2	TEST12			38	SHCLK	I	(SH) MPU clock
3	TEST13			39	VDD_01	–	[CORE] VDD
4	UPISEL0	I	I ² C slave address select	40	SHDATA0	I/O	(SH) data 0 (LSB)
5	UPISEL1		I ² C/SH interface select, L: I ² C, H: SH3	41	SHDATA1		(SH) data 1
6	TM4	I	Test configuration, connect to GND.	42	SHDATA2		(SH) data 2
7	MVSW	I	Reserved for Test	43	SHDATA3		(SH) data 3
8	VDD_00	–	[CORE] VDD	44	VDD_03	–	[PAD] VDD
9	SRN	I	System reset	45	GND_04	–	[PAD] GND
10	SCL	I	I ² C bus clock	46	SHDATA4	I/O	(SH) data 4
11	SDA	I/O	I ² C bus serial data	47	SHDATA5		(SH) data 5
12	NOSTDV	O	Non-standard & no-signal detect output	48	SHDATA6		(SH) data 6
13	CPULSE	O	Clamp pulse output	49	SHDATA7		(SH) data 7 (MSB)
14	HSYOUT	O	H sync output	50	GND_05	–	[CORE] GND
15	VSIN	I	V sync input	51	PDA0	O	Pixel data output A0
16	GND_01	–	[CORE] GND	52	PDA1		Pixel data output A1
17	CLK27I	I	External clock input (27MHz)	53	PDA2		Pixel data output A2
18	VCC_S0	–	[CORE] VCC	54	VCC_S1	–	[PAD] VCC
19	GND_S0	–	[CORE] GND	55	GND_S1	–	[PAD] GND
20	XI	I	Crystal input (27MHz)	56	PDA3	O	Pixel data output A3
21	XO	O	Crystal output (27MHz)	57	PDA4		Pixel data output A4
22	GND_03	–	[CORE] GND	58	PDA5		Pixel data output A5
23	SHCS1	I	(SH) chip select 1	59	PDA6		Pixel data output A6
24	SHCS2		(SH) chip select 2	60	VDD_04	–	[CORE] VDD
25	SHRD	I	(SH) read strobe	61	PDA7	O	Pixel data output A7
26	SHWAIT	I	(SH) wait	62	PDA8		Pixel data output A8
27	SHWR	I	(SH) write strobe	63	PDA9		Pixel data output A9
28	GND_02	I	[PAD] GND	64	GND_06	–	[PAD] GND
29	SHADR00	I	(SH) address 0 (LSB)	65	CLK27O	O	27MHz clock output
30	SHADR01		(SH) address 1	66	VDD_05	–	[PAD] VDD
31	SHADR02		(SH) address 2	67	PDB0	O	Pixel data output B0
32	SHADR03		(SH) address 3	68	PDB1		Pixel data output B1
33	SHADR04		(SH) address 4	69	PDB2		Pixel data output B2
34	SHADR05		(SH) address 5	70	PDB3		Pixel data output B3
35	SHADR06		(SH) address 6	71	GND_07	–	[PAD] GND
36	SHADR07		(SH) address 7 (MSB)	72	PDB4	O	Pixel data output B4

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
73	PDB5	O	Pixel data output B5	109	TEST07	I/O	Reserved for Test
74	PDB6		Pixel data output B6	110	TEST08		
75	PDB7		Pixel data output B7	111	SCAN_W	I	For scan test, connect to VDD.
76	VDD_06	–	[CORE] VDD	112	SCAN_T		
77	GND_08	–	[CORE] GND	113	CLKSEL	I	Clock select L: XI, H: CLK27I
78	PDB8	O	Pixel data output B8	114	TM1	I	Test configuration, connect to GND.
79	PDB9		Pixel data output B9	115	GNDA_0	–	Analog GND
80	PT0	I/O	Pixel timing signal output 0	116	VCLMPC	–	C/CbCr clamp reference voltage input
81	PT1		Pixel timing signal output 1	117	VDDA_0	–	Analog VDDA
82	PT2		Pixel timing signal output 2	118	CBIN	I	Cb signal input
83	VDD_07	–	[PAD] VDD	119	GNDA_1	–	Analog GND
84	GND_09	–	[PAD] GND	120	CRIN	I	Cr signal input
85	PT3	I/O	Pixel timing signal output 3	121	VDDA_1	–	Analog VDDA
86	PT4		Pixel timing signal output 4	122	CIN	I	Chrominance (C) signal input
87	PT5		Pixel timing signal output 5	123	GNDA_2	–	Analog GND
88	PT6		Pixel timing signal output 6	124	VRTOC	–	Decoupling capacitor connect pin for VRTOC
89	PT7		Pixel timing signal output 7	125	VRBOC	–	Decoupling capacitor connect pin for VRBOC
90	VCC_S2	–	[CORE] VCC	126	VDDA_2	–	Analog VDDA
91	GND_S2	–	[CORE] GND	127	BIAS	–	Resistor connect pin for ADC bias current
92	PT8	I/O	Pixel timing signal output 8	128	VRB	I	Bottom reference voltage input for ADC
93	PT9		Pixel timing signal output 9	129	VR1	–	Decoupling capacitor connect pin for VR1
94	ACV	O	PWM output for Y clamping reference voltage	130	VRT	I	Top reference voltage input for ADC
95	AGCP	O	PWM output for external VCA control (positive)	131	VDDA_3	–	Analog VDDA
96	AGCN	O	PWM output for external VCA control (negative)	132	GNDA_3	–	Analog GND
97	GSEL	O	GSEL control signal output	133	VRBOY	–	Decoupling capacitor connect pin for VRBOY
98	VDD_08	–	[PAD] VDD	134	VRTOY	–	Decoupling capacitor connect pin for VRTOY
99	GND_10	–	[PAD] GND	135	CVBSIN	I	CVBS/Y signal input
100	TEST00	I/O	Reserved for Test	136	VDDA_4	–	Analog VDDA
101	TEST01			137	VCLMPY	I	CVBS/Y clamp reference voltage input
102	TEST02			138	GNDA_4	–	Analog GND
103	TEST03			139	TM2	I	Test configuration, connect to GND.
104	TEST04			140	TM3		
105	TEST05			141	TEST09	I/O	Reserved for Test
106	TEST06			142	TEST10		
107	VDD_09	–	[PAD] VDD	143	VDD_10	–	[PAD] VDD
108	GND_11	–	[PAD] GND	144	GND_00	–	[PAD] GND

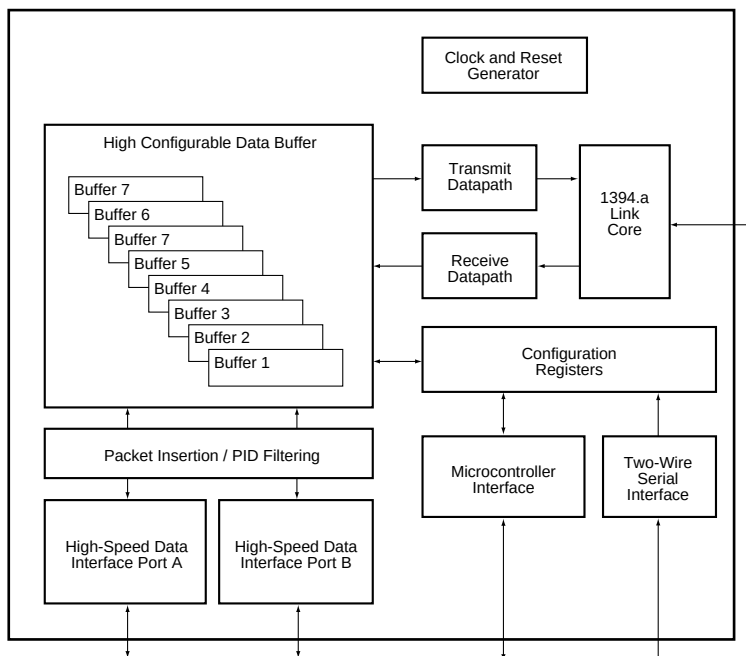
■ TSB42AB4PDT (MAIN ASSY : IC9001)

• IEEE1394 Link IC

● Pin Assignment (Top view)



● Block Diagram



● Pin Function (1/3)

No.	Pin Name	I/O	Pin Function
1	HSDIA_D7	I/O	(MSB)
2	HSDIA_D6		HSDI port A data bus
3	HSDIA_D5		
4	Vcc	–	3.3V power supply
5	HSDIA_D4	I/O	HSDI port A data bus
6	HSDIA_D3		
7	HSDIA_D2		
8	HSDIA_D1		
9	HSDIA_D0		(LSB)
10	GND	–	Ground
11	RESERVED	–	Reserved for future use Leave unconnected.
12	GPIO0	I/O	General-purpose I/O
13	HSDIA_A2	I	(MSB)
14	HSDIA_A1		HSDI port A address bus
15	HSDIA_A0		(LSB)
16	REG18_1	O	Internal 1.8V regulator output
17	REG33_1	I	Internal voltage regulator input
18	HSDIA_CLK	I	HSDI port A clock (Data is clocked on the rising clock edge.)
19	GND	–	Ground
20	HSDIA_R/XW	I	HSDI port A read/write signal Used to indicate either a host read or a host write transaction to the HSDIA port.
21	HSDIA_EN	I	HSDIA port access enable Used to indicate valid data for 1394 transmit (host writer) or 1394 receive (host read) operations.
22	HSDIA_AV	O	HSDI port A data available Used during 1394 receive operations.
23	HSDIA_SYNC	I/O	HSDI port A synchronization signal Used to determine data packet boundaries.
24	GPIO1	I/O	General-purpose I/O
25	GPIO2		
26	Vcc	–	3.3V power supply
27	JTAG_TRST	I	JTAG test reset
28	GND	–	Ground
29	JTAG_TMS	I	JTAG test mode select
30	JTAG_TCK	I	JTAG clock
31	JTAG_TDO	O	JTAG data output
32	JTAG_TDI	I	JTAG data input
33	GPIO3	I/O	General-purpose I/O
34	XMCIIF_STRB	I	Data strobe signal
35	MCIF_RW	I	Read/write indicator Indicates whether the current pending access is a read or a write.
36	XMCIIF_S32	I	Data transfer size indicator Indicates whether the host controller desires 16-bit or 32-bit transactions.
37	XMCIIF_CS	I	CeLynx chip select
38	XMCIIF_ACK	O	Acknowledge signal Indicates to the host controller the completion of the current read or write access.
39	Vcc	–	3.3V power supply
40	XRESET	I	Reset input This signal is active low.
41	GND	–	Ground
42	XINT	O	Interrupt This is the ceLynx interrupt output to the host.

● Pin Function (2/3)

No.	Pin Name	I/O	Pin Function
43	RESERVED	–	Reserved for future use Leave unconnected.
44	MCIF_D15	I/O	(MSB) Microcontroller interface bidirectional data bus
45	MCIF_D14		
46	MCIF_D13		
47	REG18_2	O	Internal 1.8V regulator output
48	REG33_2	I	Internal voltage regulator input
49	MCIF_D12	I/O	Microcontroller interface bidirectional data bus
50	MCIF_D11		
51	MCIF_D10		
52	MCIF_D9		
53	MCIF_D8		
54	GND	–	Ground
55	MCIF_D7	I/O	Microcontroller interface bidirectional data bus
56	MCIF_D6		
57	MCIF_D5		
58	MCIF_D4		
59	Vcc	–	3.3V power supply
60	MCIF_D3	I/O	Microcontroller interface bidirectional data bus (LSB)
61	MCIF_D2		
62	MCIF_D1		
63	MCIF_D0		
64	GND	–	Ground
65	MCIF_A9	I	(MSB) Microcontroller interface address bus
66	MCIF_A8		
67	MCIF_A7		
68	MCIF_A6		
69	Vcc	–	3.3V power supply
70	NCIF_A5	I	Microcontroller interface address bus (LSB)
71	MCIF_A4		
72	MCIF_A3		
73	MCIF_A2		
74	MCIF_A1		
75	GND	–	Ground
76	GPIO4	I/O	General-purpose I/O
77	PLI_CNTDR	I/O	Contender signal
78	RESERVED	–	Reserved for future use Leave unconnected.
79	XEN	I	Internal power supply enable Active low.
80	REG18_3	O	Internal 1.8V regulator output
81	REG33_3	I	Internal voltage regulator input
82	PLI_D7	I/O	(LSB) PHY-link data bus
83	PLI_D6		
84	PLI_D5		

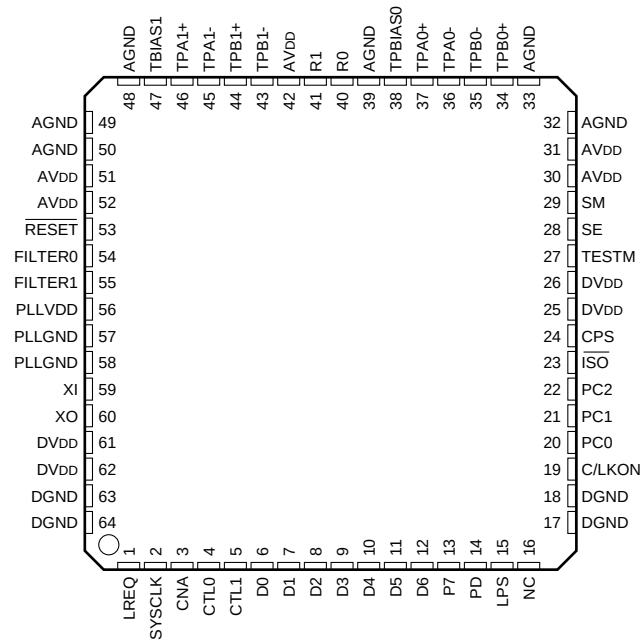
● Pin Function (3/3)

No.	Pin Name	I/O	Pin Function
85	PLI_D4	I/O	PHY-link data bus
86	PLI_D3		
87	GND	–	Ground
88	PLI_D2	I/O	PHY-link data bus (MSB)
89	PLI_D1		
90	PLI_D0		
91	PLI_CTL1	I/O	(LSB) PHY-link interface control signals (MSB)
92	PLI_CTL0		
93	Vcc	–	3.3V power supply
94	PLI_SCLK	I	Physical layer system clock Supplied by the physical layer device and is 49.125MHz. PLI_SCLK is required for link layer operation.
95	GND	–	Ground
96	PLI_LREQ	O	Link request Requests the physical layer controller to perform some service.
97	GPIO5	I/O	General-purpose I/O
98	GPIO6		
99	GPIO7		
100	Vcc	–	3.3V power supply
101	GPIO8	I/O	General-purpose I/O
102	GPIO9		
103	TESTMODE	I	Factory test pin Connect to GND for normal device operation.
104	GND	–	Ground
105	HSDIB_D7	I/O	(MSB) HSDI port B data bus
106	HSDIB_D6		
107	HSDIB_D5		
108	HSDIB_D4		
109	Vcc	–	3.3V power supply
110	HSDIB_D3	I/O	HSDI port B data bus (LSB)
111	HSDIB_D2		
112	HSDIB_D1		
113	HSDIB_D0		
114	RESERVED	–	Reserved for future use Leave unconnected.
115	RESERVED		
116	GND	–	Ground
117	HSDIB_A2	I	(MSB) HSDI port B address bus (LSB)
118	HSDIB_A1		
119	HSDIB_A0		
120	HSDIB_R/XW	I	HSDI port B read/write signal Used to indicate either a host read or a host write transaction to the HSDIB port.
121	HSDIB_EN	I	HSDIB port access enable Used to indicate valid data for 1394 transmit (host writer) or 1394 receive (host read) operations.
122	Vcc	–	3.3V power supply
123	HSDIB_CLK	I	HSDI port B clock (Data is clocked on the rising clock edge.)
124	GND	–	Ground
125	HSDIB_SYNC	I/O	HSDI port B synchronization signal Used to determine data packet boundaries.
126	HSDIB_AV	O	HSDI port B data available Used during 1394 receive operations.
127	SDA	I	Serial interface data input signal Used during ceLynx power up and reset to auto configure CFRs.
128	SCL	O	Serial interface clock

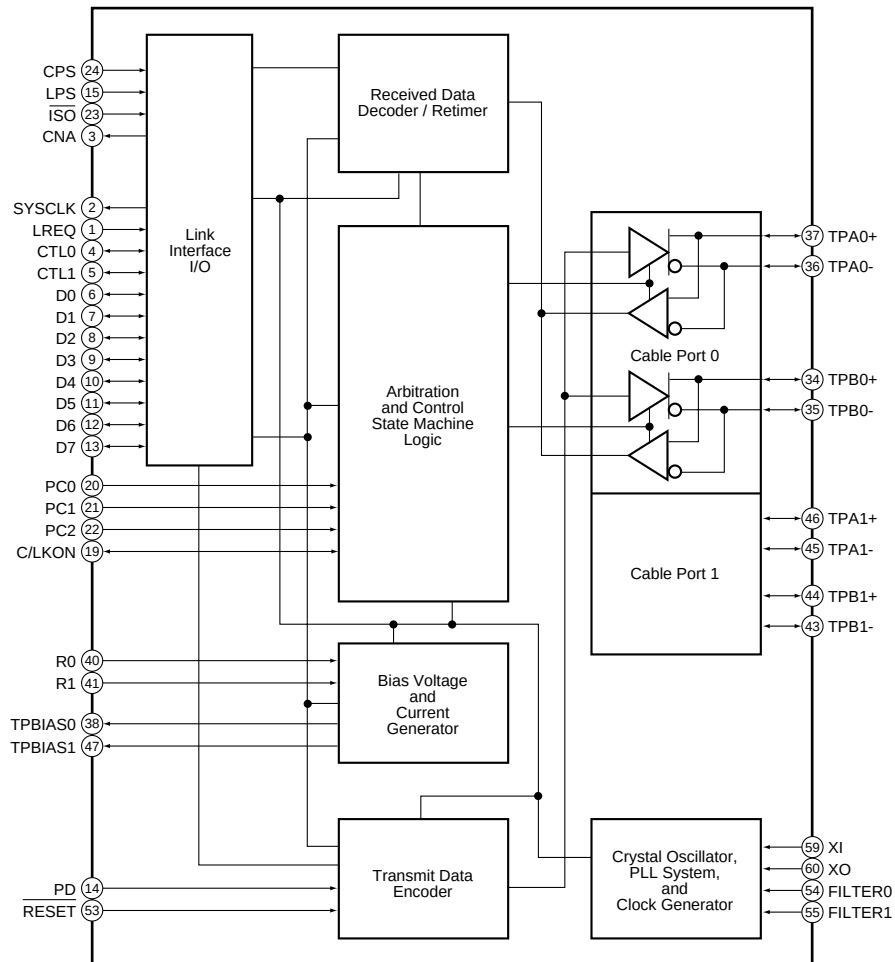
■ TSB41AB2PAP (MAIN ASSY : IC9002)

• IEEE1394 Physical IC

● Pin Assignment (Top view)



● Block Diagram



● Pin Function

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
1	LREQ	I	LLC request input The LLC uses this input to initiate a service request to the TSB41AB2.	33	AGND	–	Analog ground
2	SYSCLK	O	System clock output (49.152MHz)	34	TPB0-	I/O	Twisted-pair cable B differential signal
3	CNA	O	Cable-not-active input This pin is asserted high when there are no ports receiving incoming bias voltage.	35	TPB0+		
4	CTL0	I/O	Control I/Os These bidirectional signals control communication between the TSB41AB2 and the LLC.	36	TPA0-	I/O	Twisted-pair cable A differential signal
5	CTL1			37	TPA0+		
6	D0	I/O	Data I/Os These are bidirectional data signals between the TSB41AB2 and the LLC.	38	TPBIAS0	I/O	Twisted-pair bias output
7	D1			39	AGND	–	Analog ground
8	D2			40	R0	–	For current setting resistor
9	D3			41	R1		
10	D4			42	AVDD	–	Analog power supply
11	D5			43	TPB1-	I/O	Twisted-pair cable B differential signal
12	D6			44	TPB1+		
13	D7			45	TPA1-	I/O	Twisted-pair cable A differential signal
14	PD	I	Power down input	46	TPA1+		
15	LPS	I	Link power status input	47	TPBIAS1	I/O	Twisted-pair bias output
16	NC	–	Not used	48	AGND	–	Analog ground
17	DGND	–	Digital ground	49	AGND		
18	DGND			50	AGND		
19	C/LKON	I/O	Bus manager contender programming input and link-on output	51	AVDD	–	Analog power supply
20	PC0	I	Power class programming inputs	52	AVDD		
21	PC1			53	XRESET	I	Logic reset input
22	PC2			54	FILTER0	I/O	PLL filter
23	XISO	I	Link interface isolation control input	55	FILTER1		
24	CPS	I	Cable power status input This circuit drives an internal comparator that is used to detect the presence of cable power.	56	PLLVD	–	PLL circuit power supply
25	DVDD	–	Digital power supply	57	PLLGND	–	PLL circuit ground
26	DVDD			58	PLLGND		
27	TESTM	I	Test control input	59	XI	–	Crystal oscillator inputs
28	SE			60	XO		
29	SM			61	DVDD	–	Digital power supply
30	AVDD	–	Analog power supply	62	DVDD		
31	AVDD			63	DGND	–	Digital ground
32	AGND	–	Analog ground	64	DGND		

PE7003B (MAIN ASSY : IC9501)

• DMA I/F LSI

• Pin Function (1/2)

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
1	SCANEN	I	For ATPG (Pull-down normally)	43	TESTFNC8		
2	ATPQEN	I	For ATPG (Pull-down normally)	44	TESTFNC9		
3	Vss	–	GND	45	REQDI	O	Input REQ
4	VDD	–	3.3V power supply	46	Vss	–	GND
5	RESET	I	Reset	47	VDD	–	3.3V power supply
6	TEST_MON0	O	Test monitor output 0	48	ACKDI	I	Input ACK
7	TEST_MON1	O	Test monitor output 1	49	DATADI0	I	Input data 0
8	NEW_CLKIN	I	Input/output CLK	50	DATADI1	I	Input data 1
9	NEW_GND	–	GND	51	DATADI2	I	Input data 2
10	TEST_MON2	O	Test monitor output 2	52	DATADI3	I	Input data 3
11	TEST_MON3	O	Test monitor output 3	53	DATADI4	I	Input data 4
12	REQEI_0	O	Don't use	54	DATADI5	I	Input data 5
13	ACEKI_1	O	Input REQ	55	DATADI6	I	Input data 6
14	Vss	–	GND	56	DATADI7	I	Input data 7
15	VDD	–	3.3V power supply	57	Vss	–	GND
16	TEST_MON4	O	Test monitor output 4	58	VDD	–	3.3V power supply
17	REQEI_1	I	Input REQ	59	TESTFNC10		
18	RWEI	I	Don't use (Pull-up)	60	TESTFNC11		
19	DATAEI_0	I	Input data 0	61	TESTFNC12		
20	DATAEI_1	I	Input data 1	62	TESTIN0	I	Test input 0
21	DATAEI_2	I	Input data 2	63	TESTIN1	I	Test input 1
22	DATAEI_3	I	Input data 3	64	IRQ	O	IRQ (Interrupt Request) signal output
23	DATAEI_4	I	Input data 4	65	D0	I/O	Data bus 0
24	DATAEI_5	I	Input data 5	66	D1	I/O	Data bus 1
25	DATAEI_6	I	Input data 6	67	Vss	–	GND
26	DATAEI_7	I	Input data 7	68	VDD	–	3.3V power supply
27	Vss	–	GND	69	D2	I/O	Data bus 2
28	VDD	–	3.3V power supply	70	D3	I/O	Data bus 3
29	CLK_EO	I	Input/output CLK	71	D4	I/O	Data bus 4
30	PIN30	I	Not used	72	D5	I/O	Data bus 5
31	PIN31	I	Not used	73	D6	I/O	Data bus 6
32	TESTRAM	I	For RAM test	74	D7	I/O	Data bus 7
33	TESTNC0	I		75	Vss	–	GND
34	TESTNC1	I		76	REQEO_0	I	Don't use (Pull-up)
35	Vss	–	GND	77	REQEO_1	I	Output ACK
36	VDD	–	3.3V power supply	78	Vss	–	GND
37	TEST_MO	I	Test mode switch 0	79	VDD	–	3.3V power supply
38	TESTMI	I	Test mode switch 1	80	ACEKO_0	O	Don't use (Pull-up)
39	TESTFNC4			81	ACEKO_1	O	Output REQ
40	TESTFNC5			82	RWEO	O	Don't use (Pull-up)
41	TESTFNC6			83	DATAEO0	O	Output data 0
42	TESTFNC7			84	DATAEO1	O	Output data 1

● Pin Function (2/2)

No.	Pin Name	I/O	Pin Function
85	DATAEO2	O	Output data 2
86	DATAEO3	O	Output data 3
87	DATAEO4	O	Output data 4
88	DATAEO5	O	Output data 5
89	DATAEO6	O	Output data 6
90	DATAEO7	O	Output data 7
91	Vss	–	GND
92	VDD	–	3.3V power supply
93	A0	I	Address bus 0
94	A1	I	Address bus 1
95	A2	I	Address bus 2
96	A3	I	Address bus 3
97	A4	I	Address bus 4
98	A5	I	Address bus 5
99	Vss	–	GND
100	VDD	–	3.3V power supply
101	A6	I	Address bus 6
102	A7	I	Address bus 7
103	RD	I	RD (CPU)
104	WR	I	WR (CPU)
105	CS	I	CS (CPU)
106	CLK	I	Master CLK
107	Vss	–	GND
108	REQDO1	I	Output REQ
109	REQDO2	I	Don't use (Pull-down)
110	Vss	–	GND
111	VDD	–	3.3V power supply
112	ACKDO	O	Output ACK
113	DATADO0	O	Output data 0
114	DATADO1	O	Output data 1
115	DATADO2	O	Output data 2
116	DATADO3	O	Output data 3
117	DATADO4	O	Output data 4
118	DATADO5	O	Output data 5
119	DATADO6	O	Output data 6
120	DATADO7	O	Output data 7
121	Vss	–	GND
122	VDD	–	3.3V power supply
123	TSTEN	–	Not used
124	TCK	I	Not used (Pull-up)
125	TDI	I	Not used (Pull-up)
126	TMS	I	Not used (Pull-up)
127	TDO	O	Not used (Connection prohibition)
128	TRST	I	Not used (Pull-up)

PDY078A (MAIN ASSY : IC9503)

• CMOS EPLD

• Pin Function (1/2)

No.	Pin Name	I/O	Pin Function	Connection Point	No.	Pin Name	I/O	Pin Function	Connection Point
1	OUREMP	I	FIFO empty flag	PE7003B	33	GND	–	GND	
2	EBSACK_X	I	DMA acknowledge	PE7003B	34	VCCIO	–	VCC	
3	VCCIO	–	VCC		35	I_DATA6	O	Record system stream	IC9502
4	TDI				36	I_DATA7			
5	EBSDW0	I	Record system stream	DVxcel	37	IRDY1_X	I	Input ready	IC9502
6	EBSDW1				38	GND	–	GND	
7	EBSDW2				39	VCCINT			
8	EBSDW3				40	OEN1_X	I	Output enable	IC9502
9	EBSDW4				41	ORDY1	O	Output ready	IC9502
10	EBSDW5				42	RD_DAT_X0	O	Record system stream	IC9502
11	GND	–	GND		43	GND	–	GND	
12	EBSDW6	I	Record system stream	DVxcel	44	RD_DAT_X1	I	Record system stream	IC9502
13	EBSDW7				45	RD_DAT_X2			
14	EDMARQ	I	DMA request	DVxcel	46	RD_DAT_X3			
15	TMS				47	RD_DAT_X4			
16	AVDACK	I	DMA acknowledge	PE7003B	48	RD_DAT_X5			
17	OUMAAND	I	DMA request	PE7003B	49	RD_DAT_X6			
18	VCCIO	–	VCC		50	RD_DAT_X7			
19	ODREQ				51	VCCIO	–	VCC	
20	AVDREQ	I	DMA request	M65774AFP	52	IEN1	O	Input enable	IC9502
21	AVDREQX	O	DMA request	PE7003B	53	GND	–	GND	
22	WAITDVX	I	CPU wait	DVxcel	54	OUWMD_X0	I	Record system stream	PE7003C
23	WAITDVSH	O	DVxcel wait NG	SH3	55	OUWMD_X1			
24	LOR0	O	Read	IC9502	56	OUWMD_X2			
25	LIOW0		Write	IC9502	57	OUWMD_X3			
26	GND	–	GND		58	OUWMD_X4			
27	I_DATA0	O	Record system stream	IC9502	59	GND	–	GND	
28	I_DATA1				60	OUWMD_X5	I	Record system stream	DVxcel
29	I_DATA2				61	OUWMD_X6			
30	I_DATA3				62	TCK			
31	I_DATA4				63	OUWMD_X7	I	Record system stream	DVxcel
32	I_DATA5				64	WMOUACK	I	DMA acknowledge	PE7003B

● Pin Function (2/2)

No.	Pin Name	I/O	Pin Function	Connection Point
65	GND	–	GND	
66	VCCIO	–	VCC	
67	WMOURQ_X	I	DMA request	DVxcel
68	OUWMRQ	O	DMA request	PE7003B
69	DVFRM	I	DV frame sync	TSB42AA4PTD-5C
70	DVOEN	I	Output enable	SH3
71	XCS42	I	Chip select	PE5219A
72	LRDWR	I	Read/write	SH3
73	TDO			
74	GND	–	GND	
75	MKBRD	I	DMA flag	SH3
76	WAITWM	I	CPU wait	High level fixing
77	GPIO3_WM0	I	FIFO full flag	TSB42AA4PTD-5C
78	GND	–	GND	
79	TBCLK	O	6.75MHz clock	DVxcel
80	HSDIA_CLK	O	6.75MHz clock	TSB42AA4PTD-5C
81	27MSEL	I	27MHz clock	
82	VCCIO	–	VCC	
83	DVCSEL	I	DV I/O switch	PE5108A
84	MCIF_STRBZ	O	Strobe	TSB42AA4PTD-5C
85	MCIF_ACKZ	I	Acknowledge	TSB42AA4PTD-5C
86	GND	–	GND	
87	40MPLD	I	40MHz clock	
88	XRESET	I	Reset	
89	LXWE0	I	Write enable	SH3
90	LXRD	I	Read	SH3
91	VCCIO	–	VCC	
92	SELVR	I	VR-VIDEO select	SH3
93	LXCS56	I	Chip select	PE5219
94	HSDIA_EN	O	Request	TSB42AA4PTD-5C
95	GND	–	GND	
96	HSDIA_AV	I	Acknowledge	TSB42AA4PTD-5C
97	XWAITDV	O	CPU wait	PE5219A
98	DVACK	O	Acknowledge	DVxcel
99	DVREQ	I	Request	DVxcel
100	XWAITBY	I	CPU wait	PE5108A

• Stream Check IC

● Pin Function

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VDD	26	GND	51	VDD	76	GND
2	CLK	27	TP03	52	PO_EN1	77	TP11
3	GND	28	TP02	53	PO_RDY1	78	I_DAT7
4	LCS0	29	TP01	54	TP_SEL0	79	I_DAT6
5	TP06	30	TP00	55	RO_EN1	80	I_DAT5
6	LIOW0	31	SCK	56	RO_RDY1	81	I_DAT4
7	TP16	32	AMC	57	RO_DAT7	82	TP10
8	TP05	33	TP14	58	INT	83	I_DAT3
9	LIOR0	34	TP13	59	RO_DAT6	84	I_DAT2
10	LWAIT0	35	PO_DAT7	60	GND	85	I_DAT1
11	LDB7	36	TP12	61	RO_DAT5	86	I_DAT0
12	LDB6	37	PO_DAT6	62	RO_DAT4	87	TP09
13	TEB0	38	GND	63	VDD	88	VDD
14	LDB5	39	PO_DAT5	64	RO_DAT3	89	TP18
15	GND	40	TP_SEL4	65	RO_DAT2	90	TP17
16	LDB4	41	PO_DAT4	66	GND	91	LAB06
17	SMC	42	TP_SEL3	67	RO_DAT1	92	TP08
18	TIN	43	PO_DAT3	68	RO_DAT0	93	LAB05
19	TP04	44	TP_SEL2	69	SIMMOD0	94	LAB04
20	LDB3	45	PO_DAT2	70	I_EN1	95	LAB03
21	LDB2	46	VDD	71	I_RDY1	96	TP07
22	TP15	47	PO_DAT1	72	RST0	97	LAB02
23	LDB1	48	TP_SEL1	73	GND	98	LAB01
24	LDB0	49	PO_DAT0	74	EX_CLK	99	LAB00
25	VSS	50	GND	75	VDD	100	GND

7.3 OUTLINE OF THE PRODUCT

7.3.1 DVD-RW Standard

The DVD-RW disc is a phase-change type, rewritable disc, as are CD-RW and DVD-RAM discs. In playback of a phase-change type disc, signals that are obtained through the change in reflectivity between crystalline and amorphous states of the recording layer can be read by the optical system employed in playback-only players. Fig. 1 shows the structure of a DVD-RW disc. On a 0.6-mm-thick polycarbonate molded substrate, an Ag-In-Sb-Te-alloy recording layer, a protective layer, and a reflective layer are deposited. DVD-RW uses CLV-type groove-recording format, and employs the wobble groove & land pre-pit system, as does DVD-R, for rotation control and address information during recording. For this, so-called LPPs (Land Pre-Pits) are provided on certain locations in the land areas, and the groove has a minutely undulating structure called "wobble." The wobble is mainly used for rotation control of the disc, and the frequency of the wobble signal is 8 times that of the sync frame (8 cycles in one sync frame). LPPs are located from the first to the third bits of the sync frame at the maximum oscillation of the wobble, and these three bits and one ECC (error correction code) comprise preaddress information. Table 1 shows the basic specifications of DVD-RW. The specifications, such as the form of the disc, 4.7 GB/side recording capacity, 0.4 μm minimum pit length, 0.74 μm track pitch, modulation method, and error-correcting code, are the same as those of DVD-ROM. The recording and playback wavelengths are both 635/650 nm.

As to the characteristics after recording, the reflectivity is within the standard value of a dual-type DVD-ROM, and the specifications for modulation and jitter are the same as those of DVD-ROM format. Moreover, as the tracking system during playback, phase-difference tracking is employed, analogous to DVD-ROM.

Table 1 Basic Specifications of DVD-RW

Item	Specifications of DVD-RW	Specifications of DVD-ROM
Media Type	Phase Change Re-writable	Read Only
Diameter	120/80mm	←
Pre-format	Wobble & LPP	-----
Spindle Control	CLV	←
User Data Capacity	4.7G/1.46Gbytes	8.54Gbytes **
Recording Rate	11.08Mbps	←
Record Wave Length	635/650nm	-----
Playback Wave Length	635/650nm	←
Write Power	– 15mW	-----
Track Pitch	0.74 μm	←
Minimum Pit Length	0.4 μm	←
Data Modulation	8-16Modulation	←
Reflectivity	18 – 30 %	45-85%* 18-30%**
Case or Cartridge	Option	-----

* Single Layer Disc
** Dual Layer Disc

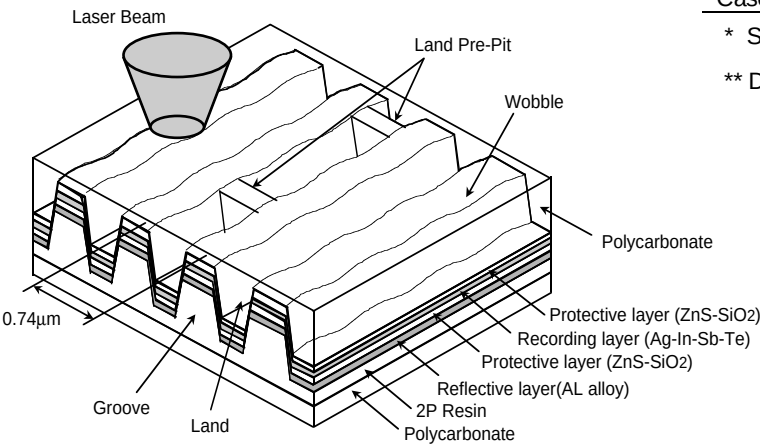


Fig. 1 Structure of DVD-RW disc

7.3.2 Video Recording Format

The DVD Forum created the DVD-Video format as an application format. As this format was created mainly for the authoring systems for a PC environment and intended to reduce the burden on playback-only players, its data structure is not suitable for real-time recording. As the DVD-Video format was for ROM discs, which do not require addition of descriptions or edition by users, its fairly complex structure posed little trouble for authoring systems. Therefore, the format contained various items that allowed content producers to use various functions, such as multiangle, multistory, various menus, multilanguage, commands, and high picture/sound quality.

In comparison, in considering the use for general users' recording/playback use, such as VCR, Camcorder, and MD, the Video Recording format was defined to respond to the following requests:

1. Real-time recording
2. Easy to edit/operate
3. High picture quality
4. Efficient usage of available area on a disc

Table 2 shows the outline of Video Recording format data.

Table 2 General Specifications of Presentation Data

Data Systems	MPEG-2 system stream / program stream Maximum program_mux_rate = 10.08Mbps			
Video	number of stream	: 1		
	compression	: Complies with MPEG-2 or MPEG-1		
	bit rate	: 9.80 Mbps or less		
	MPEG-2 MPEG-1	: 1.856 Mbps or less		
Audio	number of streams	: 2 max		
	coding mode	: Linear PCM / Dolby AC-3 / MPEG		
		Linear PCM	Dolby AC-3	MPEG-1
	sampling frequency	48kHz	48kHz	48kHz
	bits per sample	16bits	compressed	compressed
	bit rate (max.)	1.536Mbps	448 kbps	384kbps
	number of channels	2 max.	5.1 max.	2 max.
Sub-picture	number of streams	: 1 max.		
	data type	: Run-length coded bitmap , 2-bit/pixel		
	data size of a picture	: 52KB max.		
	display area	: a rectangular in a frame		
	TV system with 525 / 60	: 720(H) × 478(V) max.		
	TV system with 625 / 50	: 720(H) × 537(V) max.		
	colors	: 16 colors palette for each VOB		

Fig. 2 shows a recorded content model. The original represents an image of a group of titles previously recorded on a VCR and now actually recorded on a disc. Up to 99 titles can be recorded on a disc. A title may be actually recorded on noncontinuous areas, but for users, it appears to be recorded continuously.

The play list is a program created from time information of actual original titles, and a virtual title is composed only of management information.

Any portions of titles can be selected in any order with accuracy to one video frame in a play list. Up to 99 play lists can be created. Both original titles and play lists can contain chapters.

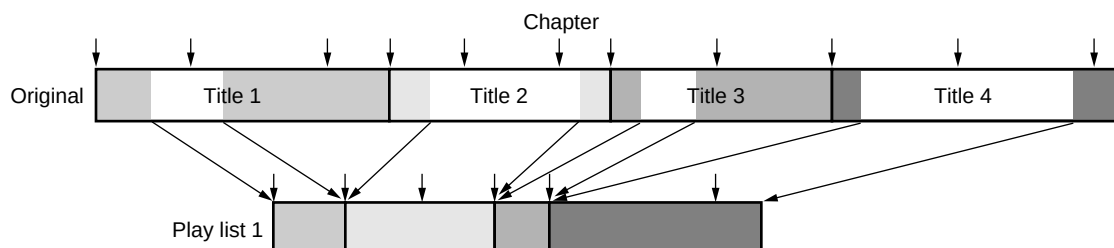


Fig. 2 Recorded content model

7.3.3 Main Newly Developed Features

7.3.3.1 Pickup

In addition to DVD-R/RW recording and DVD-ROM playback, the newly developed pickup can play back CD media. The laser diodes are provided separately for DVD and CD, but one lens is used for both.

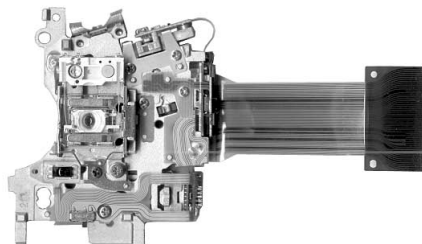


Fig. 3 Pickup

7.3.3.2 LSI for Process of Recording Signals

The conventional structure of 3 chips and a discrete circuit has been integrated into 2 chips, realizing performance stabilization and cost reduction.



RECORDER DRIVE
MAIN
IC109 PM0025AF



RECORDER DRIVE
MAIN
IC602 PE5131A

Fig. 4 A2-Chip R3-Chip

7.3.3.3 Video Decoder LSI

A video decoder LSI for high-quality conversion of analog video signals to digital signals has been newly developed. By mounting a 10-bit/27-MHz video ADC, higher accuracy and better stabilized reproduction of luminance and color have been realized.



MAIN Assy
IC8008 PD0272A

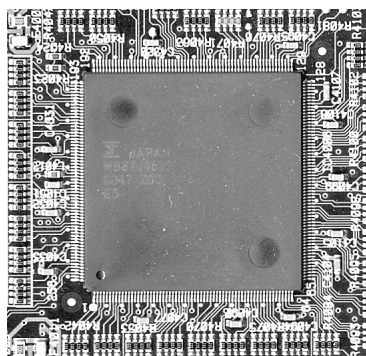
Fig. 5 George

7.3.3.4 MPEG Video Encoder LSI

A new MPEG video encoder LSI, which enables recording in 3/4-D1 and 2/3-D1 resolutions in addition to conventional full-D1 and 1/2-D1 resolutions available with the conventional MPEG-2 encoders, has been developed. This offers more options of resolutions suited to length of recording, and enables higher picture quality even with longer recording. It also reduces load on the host CPU by substituting multiplexed processing of video and audio data for it, and contributes to cost reduction by assuming the DV codec function.

7.3.3.5 Graphics Engine LSI

An LSI for graphics processing, such as full-resolution GUI and the reduced-size-moving-picture-capture function, has been newly developed for easier operation and an easy-to-understand user interface. This can dramatically improve UI expression. This LSI also has high-quality picture features, such as frame TBC (Time Base Corrector) and 3DNR (Digital Noise Reduction).



MAIN Assy
IC4006 PD6342A

Fig. 4 Vaikilt

7.3.3.6 Drive Interface LSI

Conventionally, SCSI was employed as a drive interface, and was controlled by a dedicated LSI and CPU. Transfer of data was managed by the host CPU.

Now, ATAPI has been employed as the drive interface, and a new LSI has been developed. By transferring management of data transfer to the LSI, drive-control functions have been converged to the LSI, thus reducing load on the host CPU and contributing to cost reduction.



MAIN Assy
IC3003 PE5219A

Fig. 7 Slalom

7.3.3.7 LPCM Audio Recording

The DDCE (Dolby Digital Consumer Encoder) has been conventionally employed for audio encoding, and now LPCM (Linear PCM) audio recording has been created as an algorithm for AV encoding, enabling audio recording more faithful to the original sound.

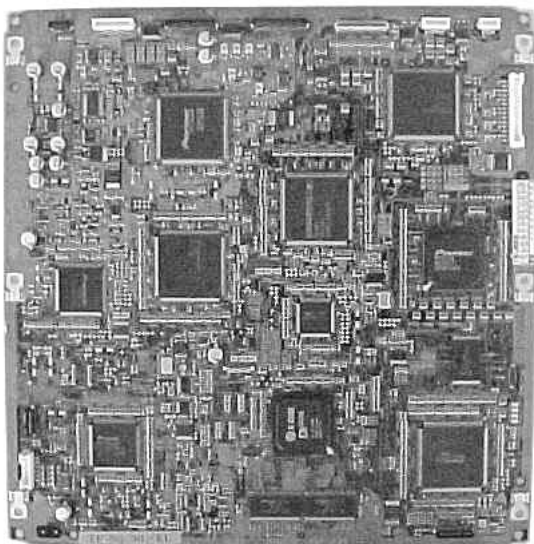


Fig. 8 MAIN Assy

7.3.4 System Control Structure

Fig. 9 shows a system block diagram of the DVR-7000. The system is roughly divided into two blocks: the writer block (which writes in and reads out data to and from a disc), and the recorder block (which encodes/decodes video and audio signals and generally controls the whole system, including UI).

7.3.4.1 Structure of the Control System

Although the DVR-2000 contained 6 CPUs, including the one controlling DV, the DVR-7000 contains the following 3 CPUs (see Fig. 10):

- (1) Recorder Main CPU
For control of the whole system, such as recording and playback operations, including control of each CPU, and user interface
- (2) Read/Write Control CPU
For control of read out/write in from/to a disc.
- (3) Tuner/FL Control CPU
For control of the tuner, FL, 3-D Y/C, and keys of the main unit, and for management of time and timer setting

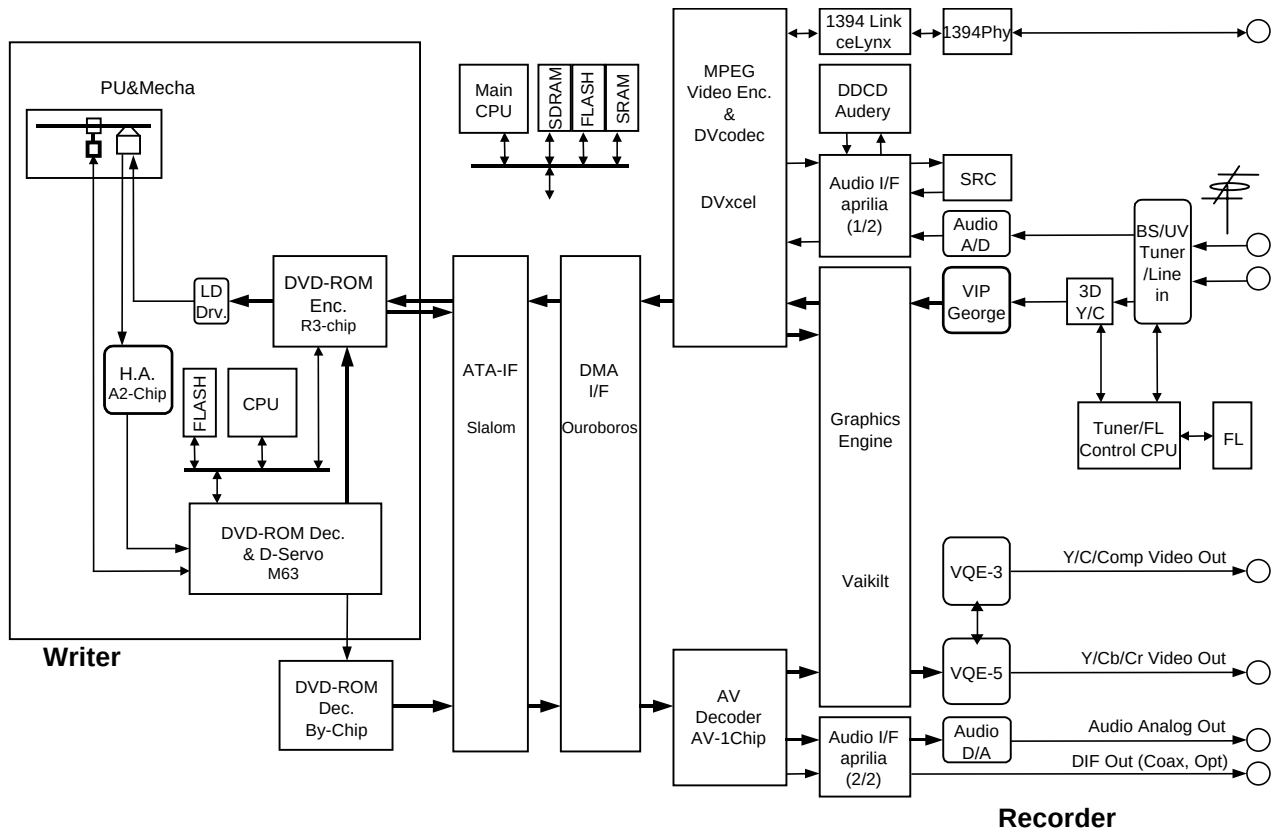


Fig. 9 System block diagram

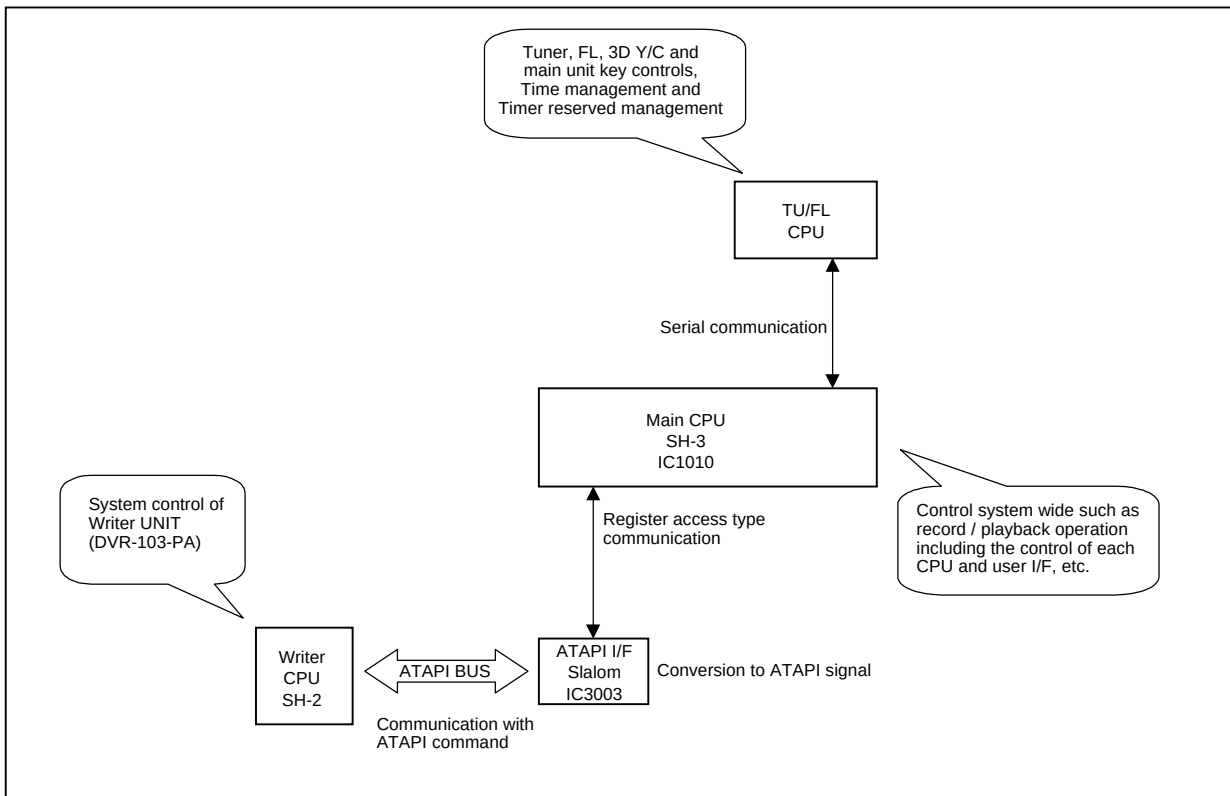


Fig. 10 CPU control share

7.3.4.2 Recording System

The basic flow of data with the DVR-7000 is similar to that with the DVR-2000. Recordable media are DVD-R (Ver. 2.0) and DVD-RW (Ver. 1.0/1.1), and recording application formats are Video Recording Format (DVD-VR) and Video Mode Recording Format. Only Video Mode Recording is possible with DVD-R discs, and DVD-VR recording is possible with DVD-RW discs (Video Mode Recording is also possible with Ver. 1.1 DVD-RW discs). The available recording speed to discs is normal speed.

In DVD-VR recording, analog video and audio line input signals or analog video and audio signals detected by the tuner are AD-converted, input to the Graphics Engine LSI, processed with the frame TBC and 3DNR, then encoded and multiplexed in real time. In the video and audio encoding block, based on the set recording length or recording bit rate, the most suitable encoding parameter is determined, and MPEG video encoding is made by variable bit rate (VBR). Compressed video stream and audio stream compressed by DDCE (Dolby Digital Consumer Encoder) are then packed and multiplexed, and are formed into a basic VOB (video object) conforming to the Video Recording Format. In the video stream, necessary information stipulated in the Video Recording Format, such as RDI (Real-time Data Information) in a VOB, is described. Everything up to this process is done by the MPEG Encoder LSI. A stream sent from this MPEG Encoder LSI is temporarily stored in the SDRAM (stream buffer) of the ATAPI interface LSI. The main CPU controls transfer so that the downstream will not overflow, and the temporarily stored stream is then transferred to the writer block via the ATAPI bus. As actual recording to a disc is done intermittently, a write command is issued when data reach certain amount, and a mass of data are transferred simultaneously.

The data is formatted into the DVD physical format in the DVD-ROM encoder of the writer block, then actually recorded on a disc with the most suitable emission power of the laser diode and the strategy. On the disc, data are recorded intermittently in blocks, and these data blocks are linked with no linking loss.

In actual operation, one title is created by one sequence of a user's starting recording through stopping recording. If recording is paused, a chapter will be created. If the disc is removed from the unit, the management information (file system and VR_MANGR.IFO, etc.), which is managed by the main CPU and which is necessary to play back the recorded video and audio signals, will be recorded on the disc. Editing can be made on the originals and play lists. For editing of a play list, only management information is updated and rewritten, and VOBs are not rewritten. Thus, nondestructive editing is possible.

7.3.5 Playback System

7.3.5.1 DVD Playback

The path for transferring AV decoder data in the DVR-7000 has largely been modified from that of the DVR-2000.

The path of DVD-video playback is the same as that of conventional DVD-video playback: The RF signal read out from a disc is converted into NRZI (non return to zero inverse) signal after passing through the preamplifier, then is sent to the recorder block; There, the DVD physical format is decoded. Then in the AV decoder, the signal is decoded into digital video and audio data. This is basically the same path as that the DVD-video player uses to play back a DVD-video disc. The playback speed is normal speed.

During playback of a DVD-VR, the data-transfer path from the writer block is the same as that in recording (via the ATAPI bus).

The RF signal read out from a disc is processed up to DVD physical formatting in the writer block, transferred via the ATAPI bus, and is temporarily stored in the SDRAM (stream buffer) of the ATAPI interface LSI. Then, the data are transferred to the AV decoder and decoded to video and audio digital data. Thus, for DVD-VR, the same path is used for recording and playback during data transfer from the recorder to the writer blocks. The playback speed of DVD-VR is double normal speed (only for DVD-VR).

The AV-decoded data pass through the same path regardless of the applications used. The digital video signal enters the Graphics Engine LSI, where the overlay process with the GUI & OSD takes place. If a disc-navigation display is called by the user, video capture and multiscreen display processes are executed for the designated frame (random designation possible) of each title. Then, the digital video signal is processed with 3DNR in the NTSC Encode LSI to be output as an analog video signal.

As to the audio signal, audio digital data to be output as an analog signal are decoded in the AV decoder, and audio digital data to be output as a digital signal are DIF-modulated after being decoded in the AV decoder, then either signal goes to the AUDIO interface LSI, where the signal to be output as a digital signal undergoes a switching process, and for the signal to be output as an analog signal, data are gathered for the level meter and switching process is executed. The signal is then output through the DAC.

7.3.5.2 CD/Video-CD Playback

Playback of CD media is newly added for the DVR-7000. The basic data flow is similar to that of a DVD-video player. Playback speed of CD media is 4 times normal speed in CAV.

As to CD-DA playback, the RF signal read out from a disc is EFM-demodulated in the writer block. Then the signal to be output as an analog signal is sent to the recorder block as a 3-line serial signal of IEC60958 format, and the signal to be output as a digital signal is DIF-modulated in the writer block and then is sent to the recorder block.

The signal to be output as an analog signal via the Audio interface LSI enters the SRC, where the sampling rate is converted from 44.1 kHz to 48 kHz. Then, the signal enters the Audio interface LSI again, and is finally output through the DAC. The signal to be output as a digital signal also undergoes a switching process in the Audio interface LSI, and then is output as DIF.

As to Video-CD playback, as with CD-DA playback, the RF signal read out from a disc is EFM-demodulated in the writer block. Then the CD-ROM data for Video-CD is then sent to the recorder block as a 3-line serial signal of IEC60958 format, as with the signal to be output as an analog signal. In the recorder block, the data are first decoded then sent to the AV decoder, where the data are decoded into video and audio digital data. Then, the data pass and are processed in the same way as with DVD playback and are then output.

7.3.6 Newly Added Functions and Specifications

The following functions and specifications are newly added to the DVR-7000, compared with the DVR-2000.

7.3.6.1 CD/Video-CD Playback

As mentioned before, the newly developed pickup for DVD-R/RW recording, responding to two wavelengths, makes it possible to play back CD media. The basic functions are the same as those of DVD-Video players.

7.3.6.2 Progressive Output

For the video output stage, the same chip set as that for the DV-S737 is employed, and the D2 terminal is mounted to respond to the progressive output. Therefore, the same functions as with the DV-S737, such as 2-3 pull-down progressive scan and movement-adaptable-type interpolation processing functions, are provided, and the 10-bit/54-MHz video DAC is included. It also has functions such as component-frame DNR and quantum noise reduction.

7.3.6.3 Picture Creation

The Picture Creation function, which integrally controls LSIs for video input and output and settings of various NRs and which realizes the highest recording and playback picture quality by making picture-quality settings to best suit the video content, is provided. The most suitable picture-quality setting is possible with a simple operation.

7.3.6.4 Recording in 3/4-D1 and 2/3-D1 Resolution

As mentioned before, a newly developed MPEG video encoder LSI enables recording in 3/4-D1 and 2/3-D1 resolutions in addition to the conventional full-D1 and 1/2-D1 resolutions available with the conventional MPEG-2 encoders. This offers more options of resolutions suited for length of recording, and enables higher picture quality even with longer recording.

7.3.6.5 LPCM Recording

In addition to the conventionally used DDCE, LPCM recording is provided to the DVD-recorder. This enables audio recording more faithful to the original sound. LPCM recording is possible only with MN32 recording rate.

7.3.6.6 Full-resolution GUI

The newly developed Graphics Engine LSI with full-resolution GUI functions dramatically improves the power of expression. In combination with the reduced-size-moving-picture-capture function, an easy-to-operate and high-quality User Interface has been realized.

7.3.6.7 Special Playback

To improve the operability and performance as an editing machine, various special playback functions and performance are provided. Besides frame-by-frame playback in forward and reverse, special playback functions, such as 1/2-, 1/4-, 1/8-, and 1/16-time playback in forward and reverse, and reverse playback at normal speed in full resolution are possible.

7.3.7 Other Features and Specifications

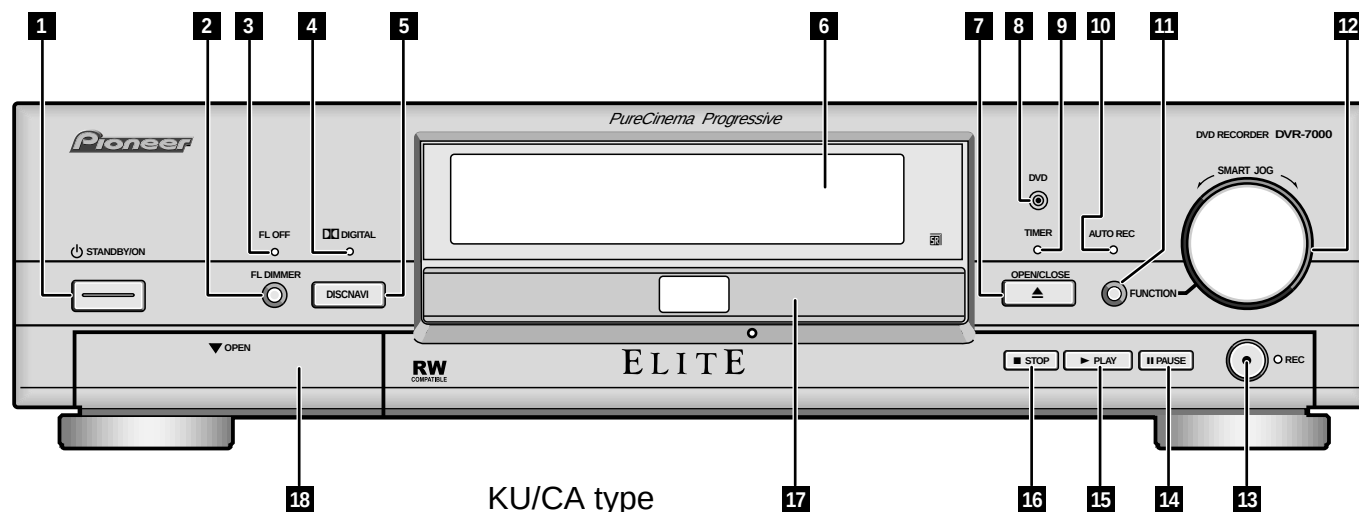
Other conventional features and specifications are as follows:

- 96-kHz/24-bit DAC
- 48-kHz/20-bit ADC
- 3-Dimensional Y/C-separation circuit
- Frame TBC
- Responding to the DV (iLink) input/output
- Built-in BS tuner
- Disc Navigator
- Disc timer
- Commercial skip

8. PANEL FACILITIES AND SPECIFICATIONS

8.1 PANEL FACILITIES

■ FRONT PANEL

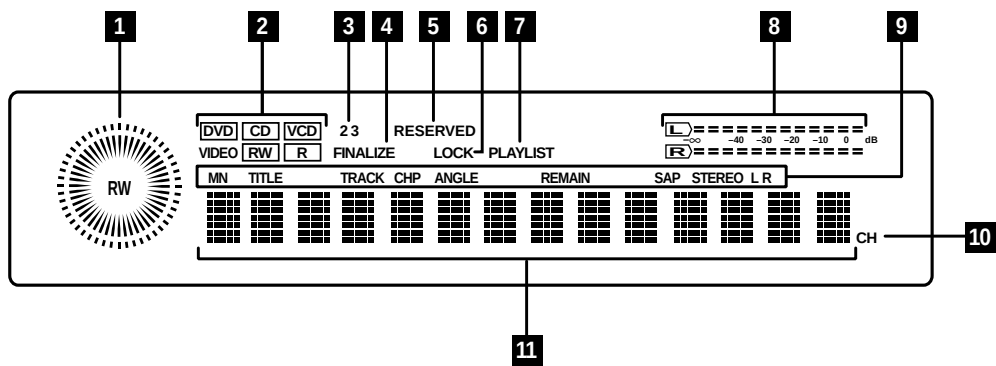


- | | |
|---|---|
| <p>1 STANDBY/ON button</p> <p>2 FL DIMMER button
Press to change the display brightness</p> <p>3 FL OFF indicator
Lights when the display is switched off using the FL DIMMER button</p> <p>4 DOLBY DIGITAL indicator
Lights when a Dolby Digital soundtrack is playing</p> <p>5 DISCNAVI button
Press to display the Discnavi screen</p> <p>6 Display</p> <p>7 OPEN/CLOSE button
Press to open/close the disc tray</p> <p>8 DVD indicator
Lights when a DVD disc is loaded</p> <p>9 TIMER indicator
Lights when the record timer is set and the power is in standby</p> <p>10 AUTO REC indicator
Lights when the recorder has been set for automatic recording</p> <p>11 FUNCTION button
Press to switch the function of the SMART JOG</p> | <p>12 SMART JOG control
Turn to change the parameter selected with the FUNCTION button</p> <p>13 REC button/indicator
Press to start recording</p> <p>14 PAUSE button
Press to pause playback or recording</p> <p>15 PLAY button
Press to start or restart playback</p> <p>16 STOP button
Press to stop playback or recording</p> <p>17 Disc tray</p> <p>18 Front panel jacks
Analog and digital input/output jacks for connecting a camcorder or other external equipment</p> |
|---|---|

RW
COMPATIBLE

This indicates a product feature that is capable of playing DVD-RW discs recorded with Video Recording format.

■ DISPLAY

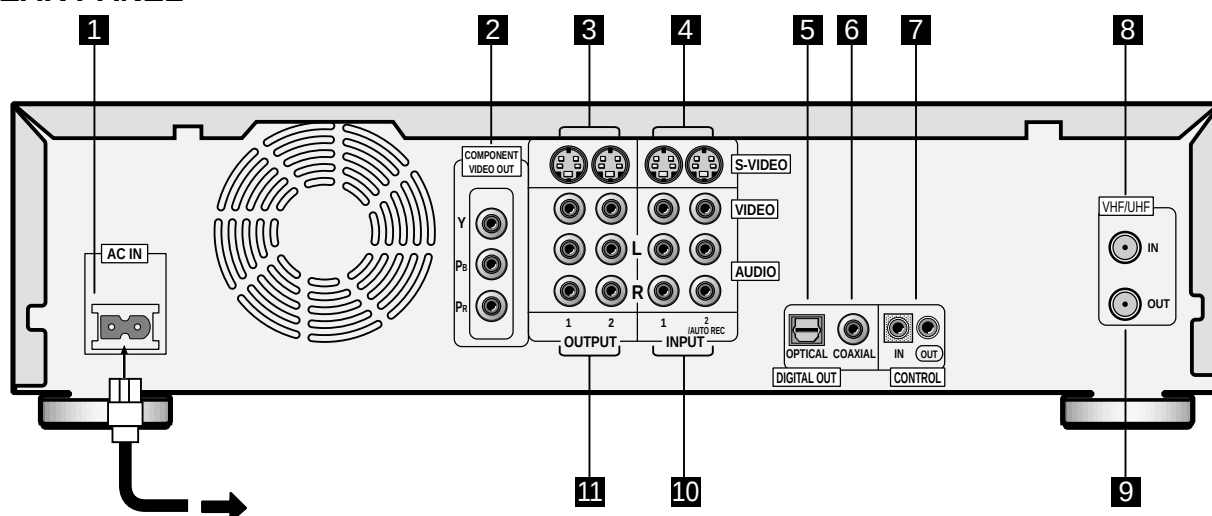


- 1 Play/record indicator
Outer (white) ring indicates the playback speed and direction. Inner (red) ring indicates elapsed playback/recording time
The center RW indicator lights when a VR mode disc is loaded
- 2 DVD CD VCD VIDEO RW R
Shows the type of disc loaded
- 3 2 3
Shows the remote control mode (if nothing is displayed, the remote control mode is 1)
- 4 FINALIZE
Lights when a finalized disc is loaded
- 5 RESERVED
Lights when a disc containing a disc timer program is loaded
- 6 LOCK
Lights when the child lock is active
- 7 PLAYLIST
Lights when a VR mode disc is loaded and the recorder is in Playlist mode
- 8 Audio level indicators
Monitors the output audio level during playback and the input audio level during recording
- 9 MN
Display shows the manual rate recording level

- TITLE
Display shows the current title number of the DVD disc playing
- TRACK
Display shows the current track number of the CD or Video CD disc playing
- CHP
Display shows the current chapter number of the DVD disc playing
- ANGLE
Lights when a multiangle scene on a DVD disc is playing, indicating that you can switch angles
- REMAIN
Display shows the amount of recording time available on the disc loaded
- SAP
Lights when the currently selected TV channel has a Secondary Audio Program channel
- STEREO
Lights when the incoming TV signal is stereo
- L R
Indicates which channels are recorded/played back when Dual Mono is selected.

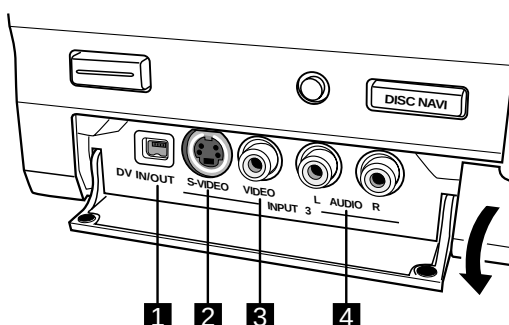
- 10 CH
Channel indicator for the built-in TV tuner
- 11 Character display

REAR PANEL



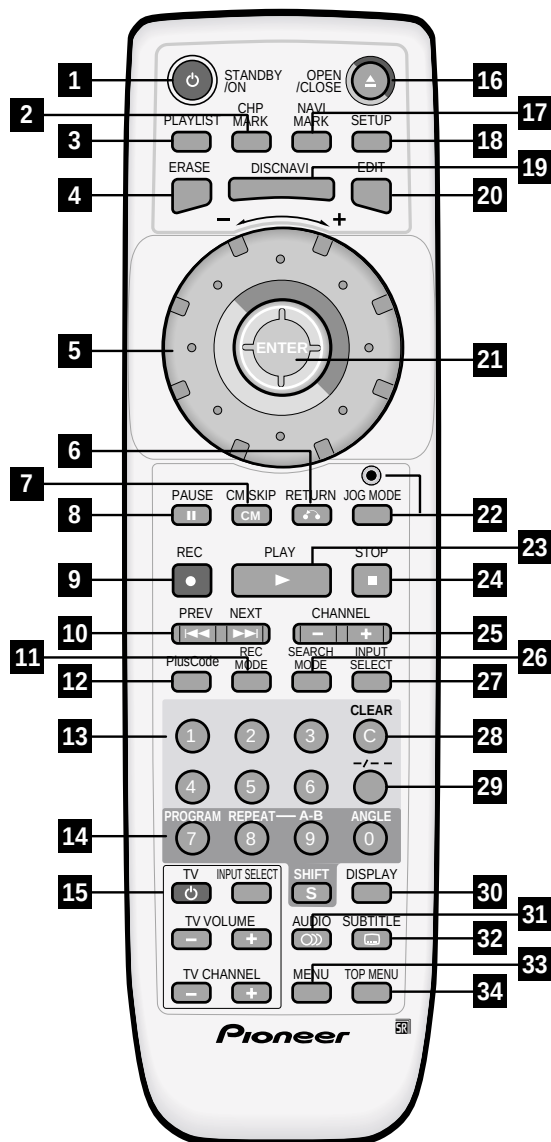
- | | |
|---|---|
| <p>1 AC IN – Power inlet</p> <p>2 COMPONENT VIDEO OUT
For connecting to a TV or monitor that has component video input</p> <p>3 S-VIDEO OUTPUT 1, 2
For connecting to a TV, monitor, AV receiver or other equipment with S-Video input</p> <p>4 S-VIDEO INPUT 1, 2
For recording from a camcorder, VCR or other equipment with S-Video output</p> <p>5 DIGITAL OUT OPTICAL
For connecting to an AV receiver, Dolby Digital/DTS decoder or other equipment with optical digital input</p> <p>6 DIGITAL OUT COAXIAL
For connecting to an AV receiver, Dolby Digital/DTS decoder or other equipment with coaxial digital input</p> | <p>7 CONTROL IN / OUT
Use for connecting to other Pioneer components bearing the Pioneer mark. Connect the CONTROL OUT of one component to the CONTROL IN of another using a mini-plug cord. The device at the beginning of the chain acts as the remote control sensor for everything in the chain.</p> <p>8 VHF/UHF IN
Connect the TV antenna here</p> <p>9 VHF/UHF OUT
Passes the signal from the VHF/UHF IN to your TV/monitor</p> <p>10 AUDIO/VIDEO INPUT 1, 2/AUTO REC
For recording from a camcorder, VCR, satellite receiver or other equipment</p> <p>11 AUDIO/VIDEO OUTPUT 1, 2
For connecting to the audio and video inputs of a TV, monitor, AV receiver or other equipment</p> |
|---|---|

FRONT TERMINAL



- | | |
|---|--|
| <p>1 DV IN/OUT jack
A combined input and output jack for connecting a digital camcorder. See page 19 for details.</p> <p>2 S-VIDEO input (INPUT 3)
Connect to an S-Video output of an external component.</p> | <p>3 VIDEO input (INPUT 3)
Connect to a composite (standard) video output of an external component.</p> <p>4 AUDIO L/R (INPUT 3)
Connect to a stereo pair of audio outputs of an external component.</p> |
|---|--|

■ REMOTE CONTROL



- 1 **STANDBY/ON**
Switches the recorder on/into standby
- 2 **CHP MARK**
Inserts a chapter marker when playing/recording a VR mode DVD-RW disc
- 3 **PLAYLIST**
Switches between Original and Playlist
- 4 **ERASE**
Shortcut to the erase function in the Discnavi or Title List screen
- 5 **Jog dial**
Controls scanning/slow motion speed and direction, and frame advance/reverse
- 6 **RETURN**
Returns to the previously displayed on-screen display
- 7 **CM SKIP**
Skips 30 seconds forward on the disc (about the length of a typical TV commercial)
- 8 **PAUSE**
Pauses playback or recording
- 9 **REC**
Starts recording. Press repeatedly to set the recording time
- 10 **PREV**
Track or chapter skip/displays the previous page of a menu

NEXT
Track or chapter skip/displays the next page of a menu
- 11 **REC MODE**
Switches the recording mode between SP to MN for a VR mode disc, or between V1 and V2 for a Video mode disc
- 12 **PlusCode (G-code for LB type)**
Press, then use the number buttons to enter a PlusCode(G-code for LB type) programming number for timer recording

- 13 **Number buttons**
- 14 **PROGRAM** (Press SHIFT first to access)
Displays the program play screen
REPEAT (Press SHIFT first to access)
Selects the repeat play mode
A-B (Press SHIFT first to access)
Marks a loop for looped playback
ANGLE (Press SHIFT first to access)
Switches camera angles on discs with multi-angle scenes
SHIFT
Press first to access the above functions
- 15 **TV controls**
Use this remote to control your TV
- 16 **▲ OPEN/CLOSE**
Opens/closes the disc tray
- 17 **NAVI MARK**
Selects a thumbnail picture for the current title for use in the Discnavi screen
- 18 **SETUP**
Displays the Setup menu
- 19 **DISCNAVI**
Displays the Discnavi screen
- 20 **EDIT**
Shortcut to the editing functions within the Discnavi or Title List screen
- 21 **Joystick / ENTER**
Use the joystick to navigate all on-screen displays. Press ENTER to select the currently highlighted option.
- 22 **JOG MODE button and indicator**
Switches the Jog dial between scanning and frame advance mode
- 23 **► PLAY**
Starts playback
- 24 **■ STOP**
Stops playback/recording
- 25 **CHANNEL -/+**
Changes the channel of the built-in TV tuner
- 26 **SEARCH MODE**
Allows searching of the disc by title, chapter, track, time, etc.
- 27 **INPUT SELECT**
Changes the input to use for recording
- 28 **CLEAR**
Clears the current setting, etc.
- 29 **-/—**
Press, then use the number button to enter a two-digit channel number
- 30 **DISPLAY**
Displays/changes the on-screen information displays
- 31 **AUDIO**
Changes the audio language or channel
- 32 **SUBTITLE**
Displays/changes the subtitles included in multilingual DVD-Video discs
- 33 **MENU**
Displays the disc menu of DVD-Video discs or the Title List screen of Video mode DVD-R/RW discs
- 34 **TOP MENU**
Displays the disc 'top' menu of DVD-Video discs or the Title List screen of Video mode DVD-R/RW discs

8.2 SPECIFICATIONS

General

System DVD-Video, DVD-R/RW, Video-CD, CD
Power requirements 120 V, 60 Hz(for KU/CA type)
Power requirements 110 V, 60 Hz(for LB type)
Power consumption 65 W
Power consumption in standby mode 1.5 W (FL off)
Weight 7.0 kg
Dimensions 420 (W) x 107 (H) x 373.5 (D) mm
Operating temperature +5°C to +35°C
Operating humidity 5% to 85% (no condensation)
TV format NTSC

Recording

Recording format DVD VideoRecording
DVD-VIDEO
Recordable discs DVD-ReRecordable
DVD-Recordable
Video recording format
Sampling frequency 13.5MHz
Compression format MPEG
Audio recording format
Sampling frequency 48kHz
Compression format Dolby Digital or Linear PCM
(uncompressed)

Recording time
DVD-RW (VR mode)
Standard (SP) Approx. 2 hours
Manual rate (MN) Approx. 1–6 hours
DVD-R/RW (Video mode)
V1 Approx. 1 hour
V2 Approx. 2 hours

Tuner

Receivable channels
VHF 1–13ch
UHF 14–69ch
CATV C1–C125ch

Timer

Programs 1 month/8 programs
Clock Quartz lock (12-hour digital display)
Power off memory Approx. 48 hours

Input/Output

VHF/UHF antenna input/output terminal VHF/UHF set
75 Ω (F-shape connector)
Video input Input 1,2 (rear), 3 (front)
Input level 1 Vp-p (75 Ω)
Jacks RCA jack
Video output Output 1,2
Output level 1 Vp-p (75 Ω)
Jacks RCA jack
S-Video input Input 1,2 (rear), 3 (front)
Y (luminance) - Input level 1 Vp-p (75 Ω)
C (color) - Input level 286 mVp-p (75 Ω)
Jacks 4 pin mini DIN
S-Video output Output 1,2
Y (luminance) - Output level 1 Vp-p (75 Ω)
C (color) - Output level 286 mVp-p (75 Ω)
Jacks 4 pin mini DIN
Component video output
Output level Y: 1.0 Vp-p (75 Ω)
P_B, P_R: 0.7 Vp-p (75 Ω)
Jacks RCA jacks
Audio input Input 1,2 (rear), 3 (front) L/R
Input level
During audio input 2V rms
(Input impedance: more than 22kΩ)
Jacks RCA jacks
Audio output Output 1,2 L/R
During audio output 2V rms
(Output impedance: less than 1.5kΩ)
Jacks RCA jacks
Control input/output Mini jack 1 each
DV input/output 4 pin (i.LINK/IEEE 1394 standard)

Supplied accessories

Remote control 1
Dry cell batteries (AA/R6P) 2
Stereo audio cable (red/white) 1
Video cable (yellow) 1
RF antenna cable 1
Power cable 1
DVD-RW disc (KU/CA type only) 1
Operating Instructions (for KU/CA type) 1
Operating Instructions (for LB type) 2
Warranty card (KU/CA type only) 1

Note: The specifications and design of this product are subject to change without notice, due to improvement.

ACCESSORIES

